Open-access silicon photonics technologies of ePIXfab members: updates 2021

Dr. Abdul Rahim

Disclaimer: The technology update information is provided by the respective foundries.

ePIXfab – the European Silicon Photonics Alliance

How do you select the right foundry?

Important questions to ask yourself (or a design house/consortium):

- Which is the best platform for my application?
- What volumes do I require?
- Is the MPW offering suitable for my application?
- Does the MPW timetable suit my schedule?
- What are the prospects for scaling up volumes?
- What are the IP terms?
- What is the most cost effective fabrication technology for my application?
- Are the standard building blocks suitable for my design?
- What level of design support do I require?

With permission from: Callum Littlejohns (Cornerstone)

How do you select the right foundry?

<u>Example: High speed transceiver prototype:</u>

1. What is the best platform for my application?
   Thin SOI

2. Which foundry offers the required functionality?
   High speed modulator and photodetector

3. Which foundry is the most cost effective for low volumes?
   MPW capability

With permission from: Callum Littlejohns (Cornerstone)

How can you benefit from the open-access community?

1. High risk device level innovation using e-beam lithography (early stage research)

2. Transfer device fabrication to DUV processes using flexible platforms (prototyping)

3. Dedicated engineering batch/s at low/medium volume foundry (manufacturing)

With permission from: Callum Littlejohns (Cornerstone)

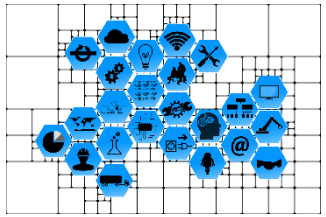
Silicon Photonics Ecosystem: Ideation to Deployment

Ideation

Markets

↓

Applications

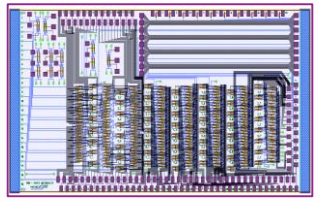


Design

Design Software

↓

Designers, Design houses



Fabrication

Wafer suppliers

↓

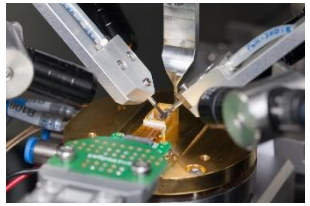
Research and technology organizations & pure-play fabs

Test, assembly, packaging

Equipment providers

↓

High- throughput test, assembly & pack. service



Deployment

Industry standards

↓

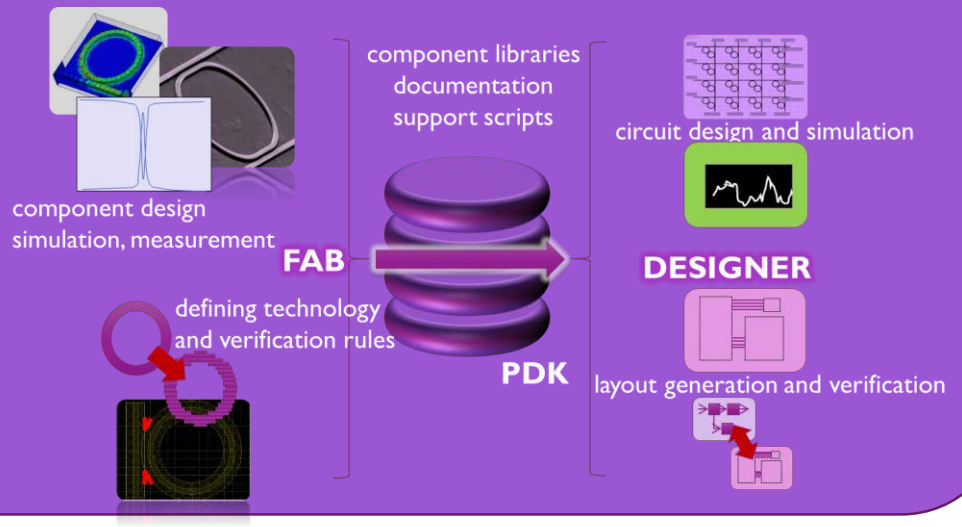
Performant in operational environment

Silicon Photonics Design

Status of Silicon Photonics Design Flow

- Physical-level design and simulation
- Circuit-level design and simulation
- System-level simulation
- Design layout and verification
- Schematic-driven layout
- Layout-vs-Schematic verification
- Co-integration of electronic and photonic designs
- Yield prediction and variability analysis

The Role of Process Design Kit (PDK)



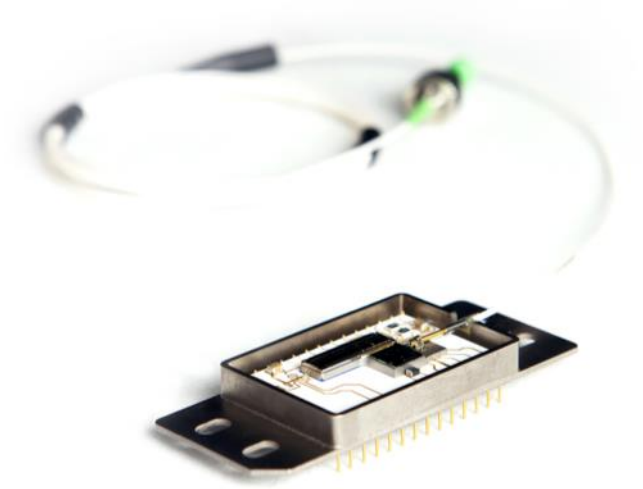
Current status of Silicon Photonics PDKs

Attribute	Definition	Electronics	Photonics
Tech. Data	Details about technology & processes		
Device library	Collection of tested building blocks		
P-cells	Parametric cells of the building blocks		
DRC	Design rule contraints		
Simulation Models	Compact models of the building blocks		
Corner Models	Impact of extremity of fabrication parameter		
Stochastic Models	Impact of stochastic fabrication tolerances		
Reliablity	Reliablity data of building blocks		

The Future of Photonic Packaging

Current

‘Gold Box’ Package



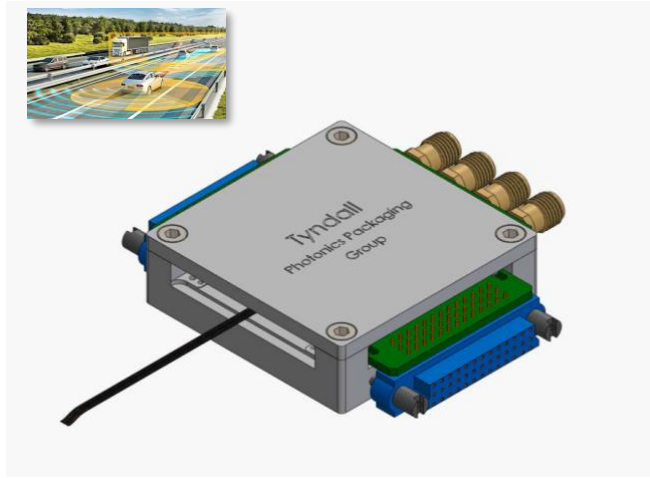
component-level packaging

PIXAPP Photonic Packaging Pilot Line

1. Pilot Scale Packaging
2. Training & Education
3. Standards & Roadmaps

Future

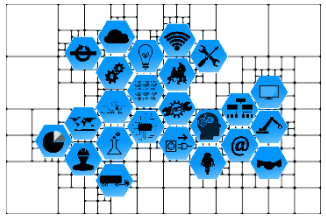
10-100 times cheaper Package

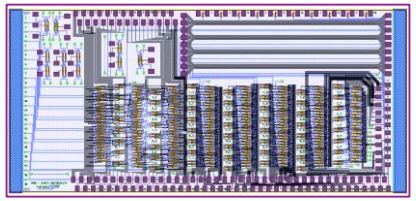


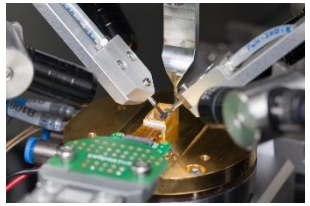
High Throughput wafer-level packaging

Silicon Photonics: Ideation to deployment

Ideation	Design	Foundry	Test, assembly, packaging	Deployment
Markets ⇩ Applications	Design Software ⇩ Designers, Design houses	Wafer suppliers ⇩ Research and technology organizations & pure-play fabs	Equipment providers ⇩ High- throughput test, assembly & pack. service	Industry standards ⇩ Performant in operational environment







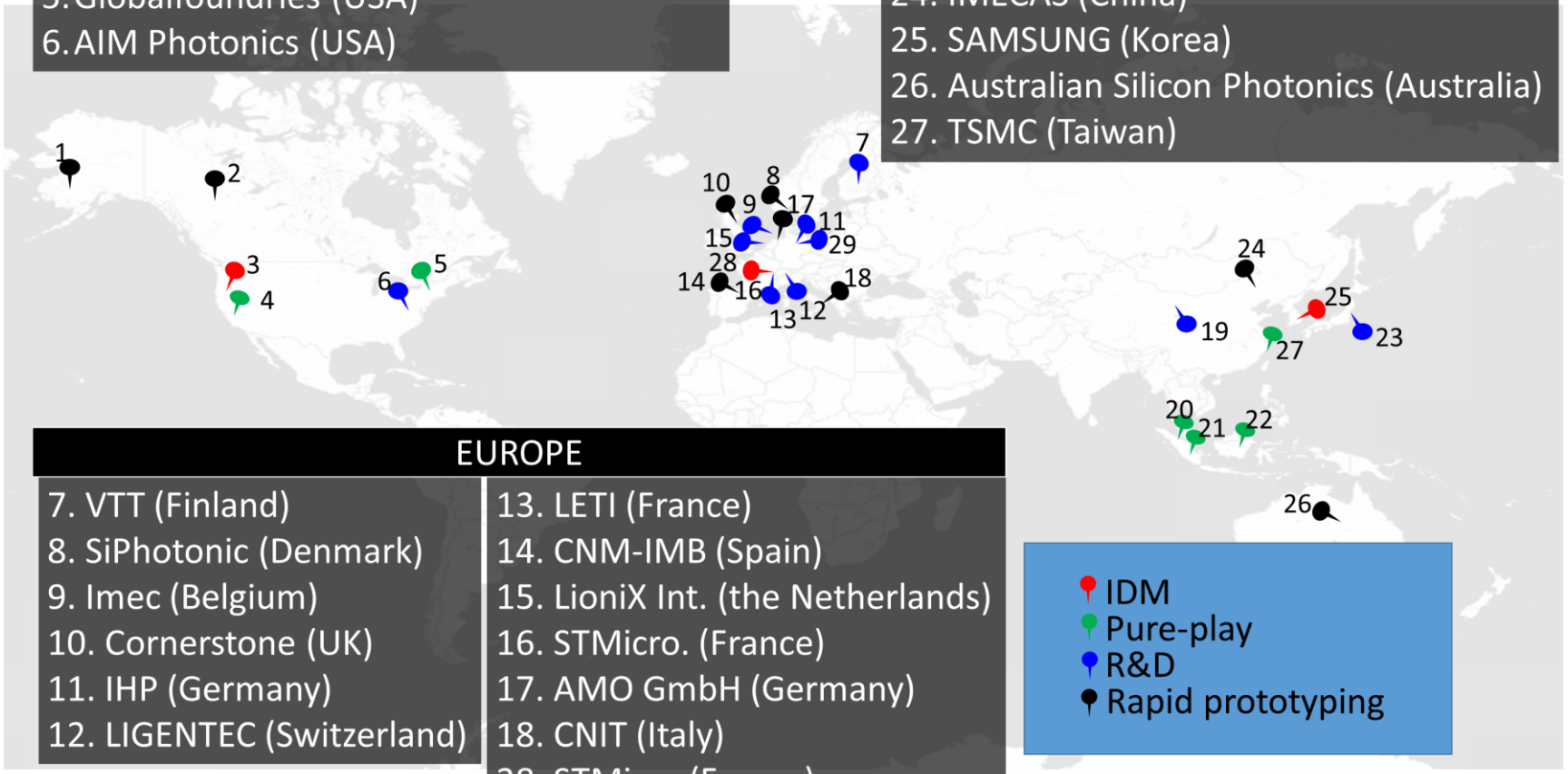
Who fabricates silicon photonics ICs?

NOERH AMERICA

1. ULL Technologies (USA)
2. Applied Nanotools Inc. (Canada)
3. Intel (USA)
4. Tower Semicon. (USA)
5. Globalfoundries (USA)
6. AIM Photonics (USA)

ASIA

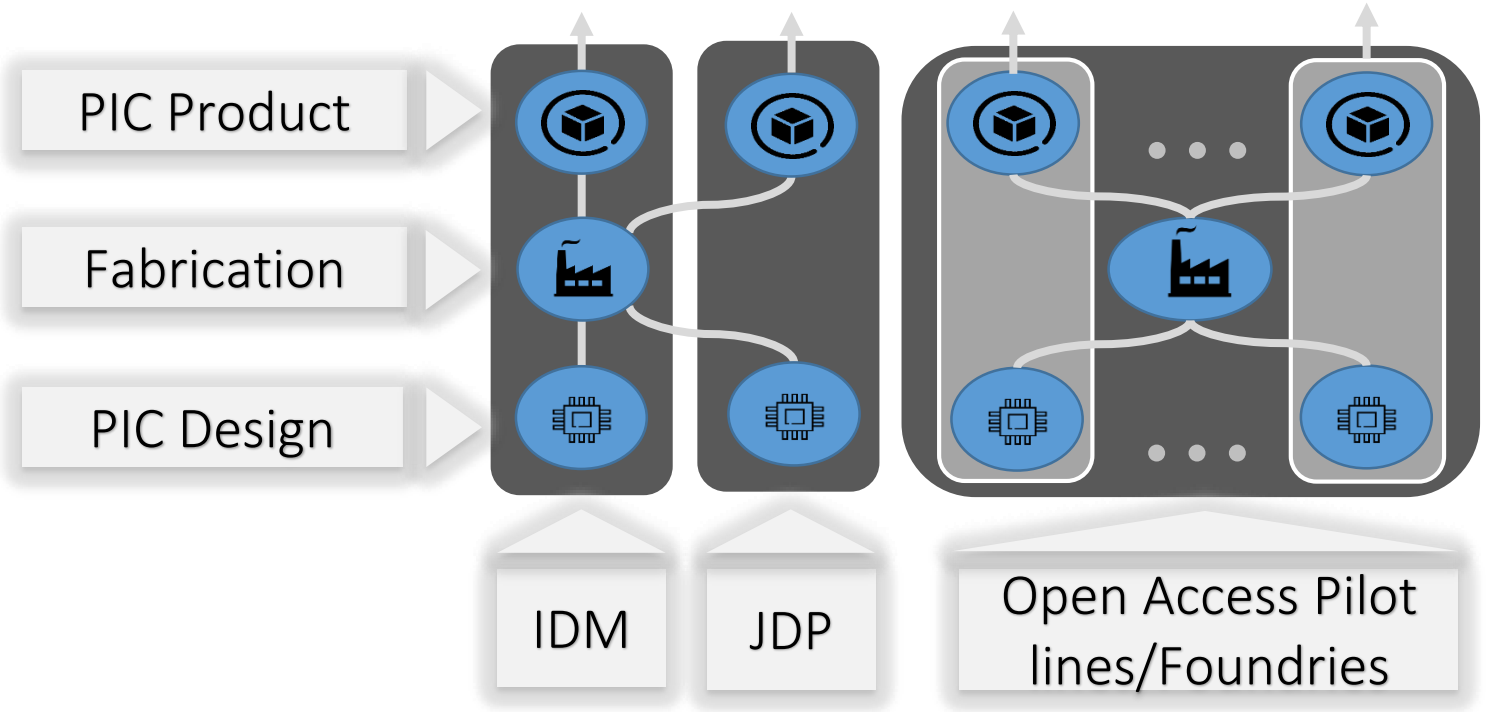
19. CUMEC (China)
20. Advanced Micro Foundry (Singapore)
21. CompoundTek (Singapore)
22. SilTerra (Malaysia)
23. PETRA (Japan)
24. IMECAS (China)
25. SAMSUNG (Korea)
26. Australian Silicon Photonics (Australia)
27. TSMC (Taiwan)



EUROPE

7. VTT (Finland)
8. SiPhotonic (Denmark)
9. Imec (Belgium)
10. Cornerstone (UK)
11. IHP (Germany)
12. LIGENTEC (Switzerland)
13. LETI (France)
14. CNM-IMB (Spain)
15. LioniX Int. (the Netherlands)
16. STMicro. (France)
17. AMO GmbH (Germany)
18. CNIT (Italy)
28. STMicro (France)
29. Bosch (Germany)

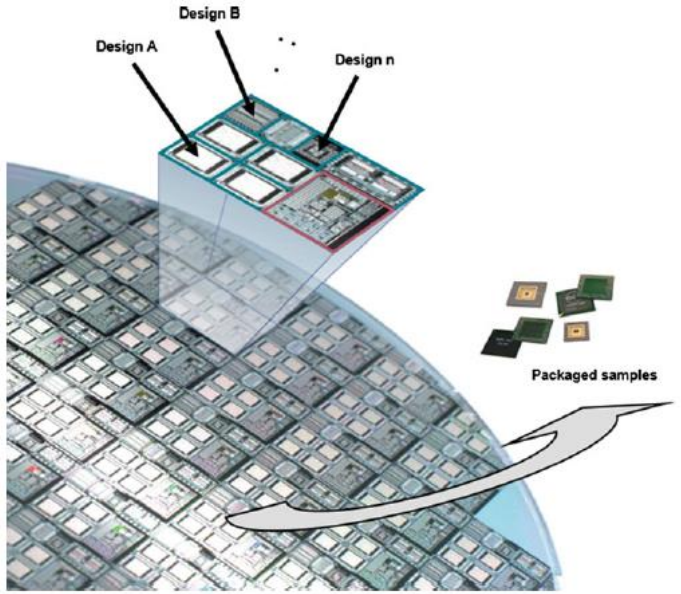
Access Models for Silicon Photonics ICs

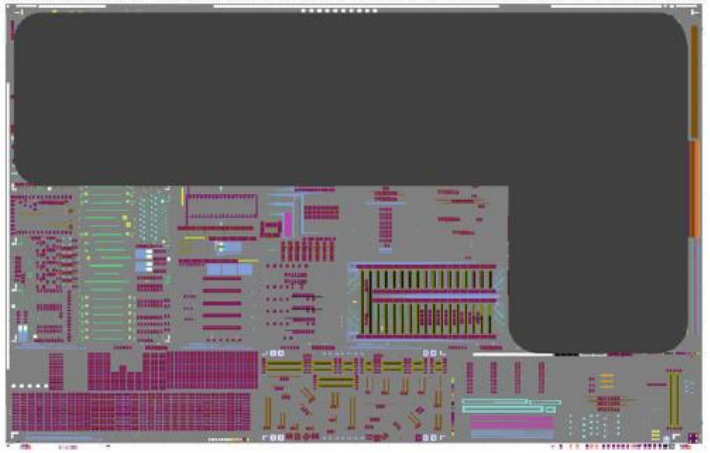


- Open access
  - a model that offers fabrication services to third parties, i.e., to external users /clients outside of a technology consortium
  - Generally used by fabless companies to get access to a technology

Open-access modes

- Multi-project Wafer (MPW) runs
  - For proof-of-concept and early stage R&D
  - Cost sharing among various users
  - Uses standardized technology
  - 4 to 9 months turn-around times
- Dedicated Engineering Runs
  - Avoids economic burden of optimizing custom building blocks
  - Large design space to put design sweeps for optimizing
  - Standardized or customized process flow
- Pre-production runs
- Volume Manufacturing

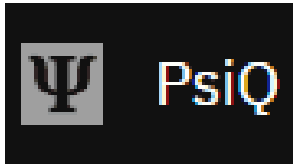




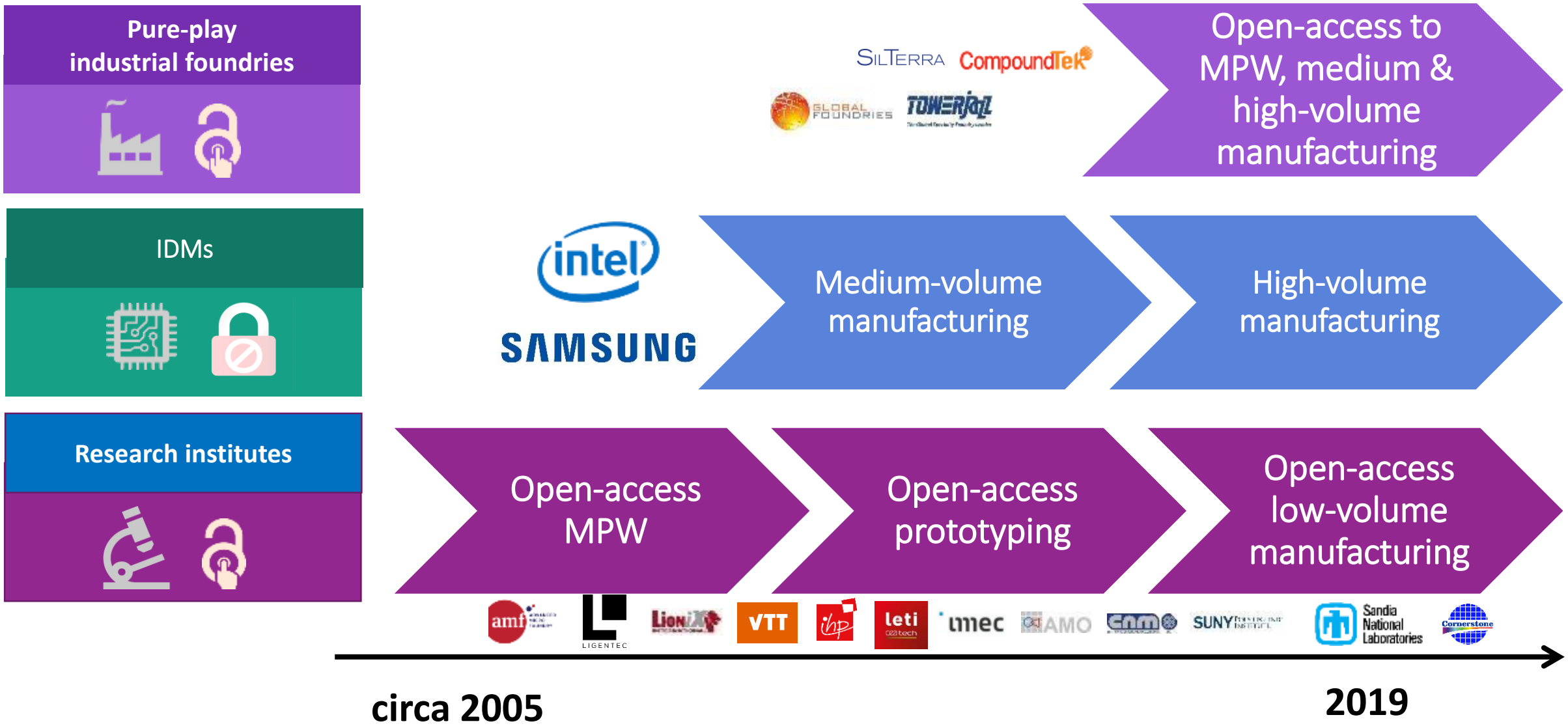
Why is open-access important?

Not exhaustive

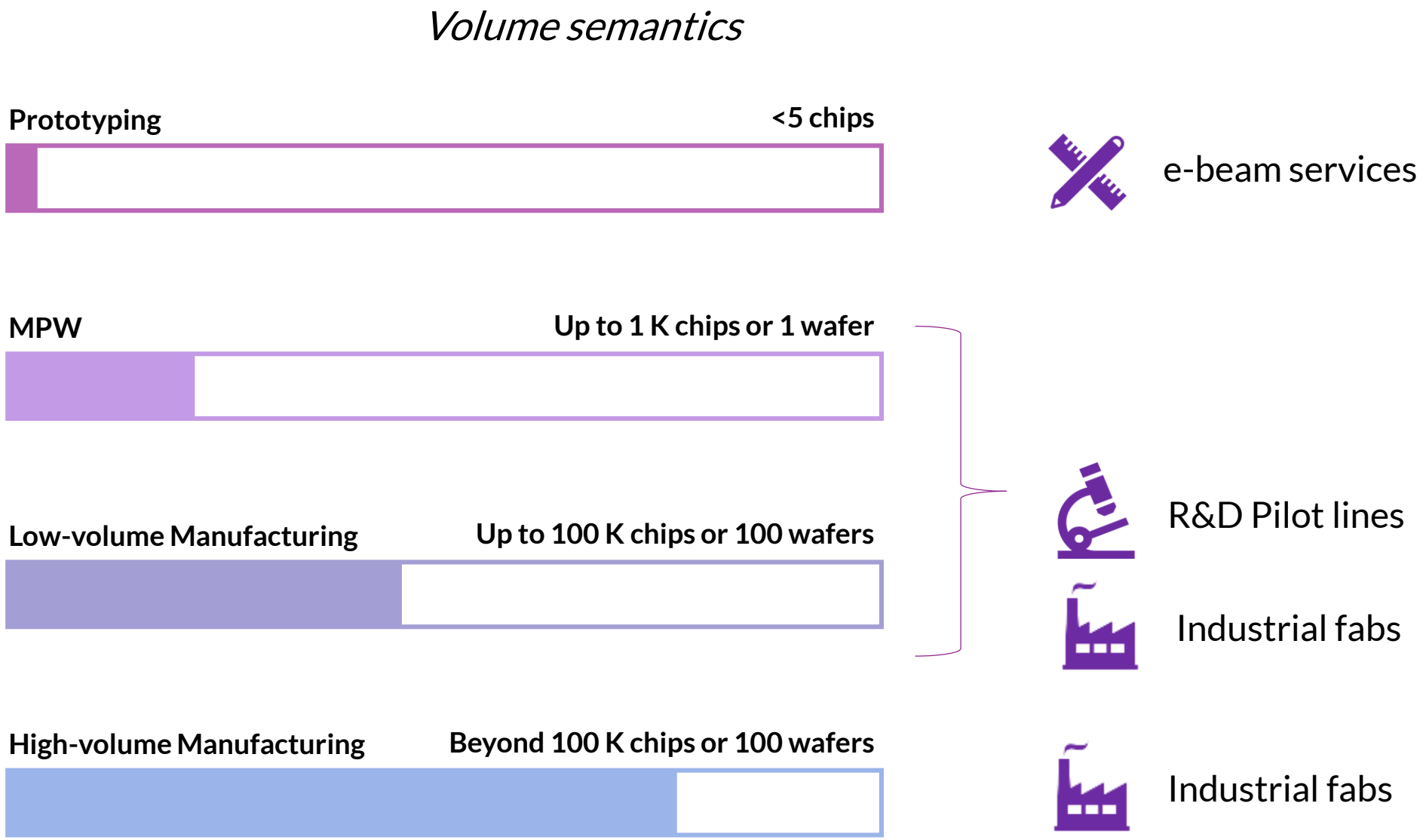
- Optical communication
- Biomedical sensors
- Autonomous vehicles
- Industrial sensors
- Quantum computing
- Aeronautics and space



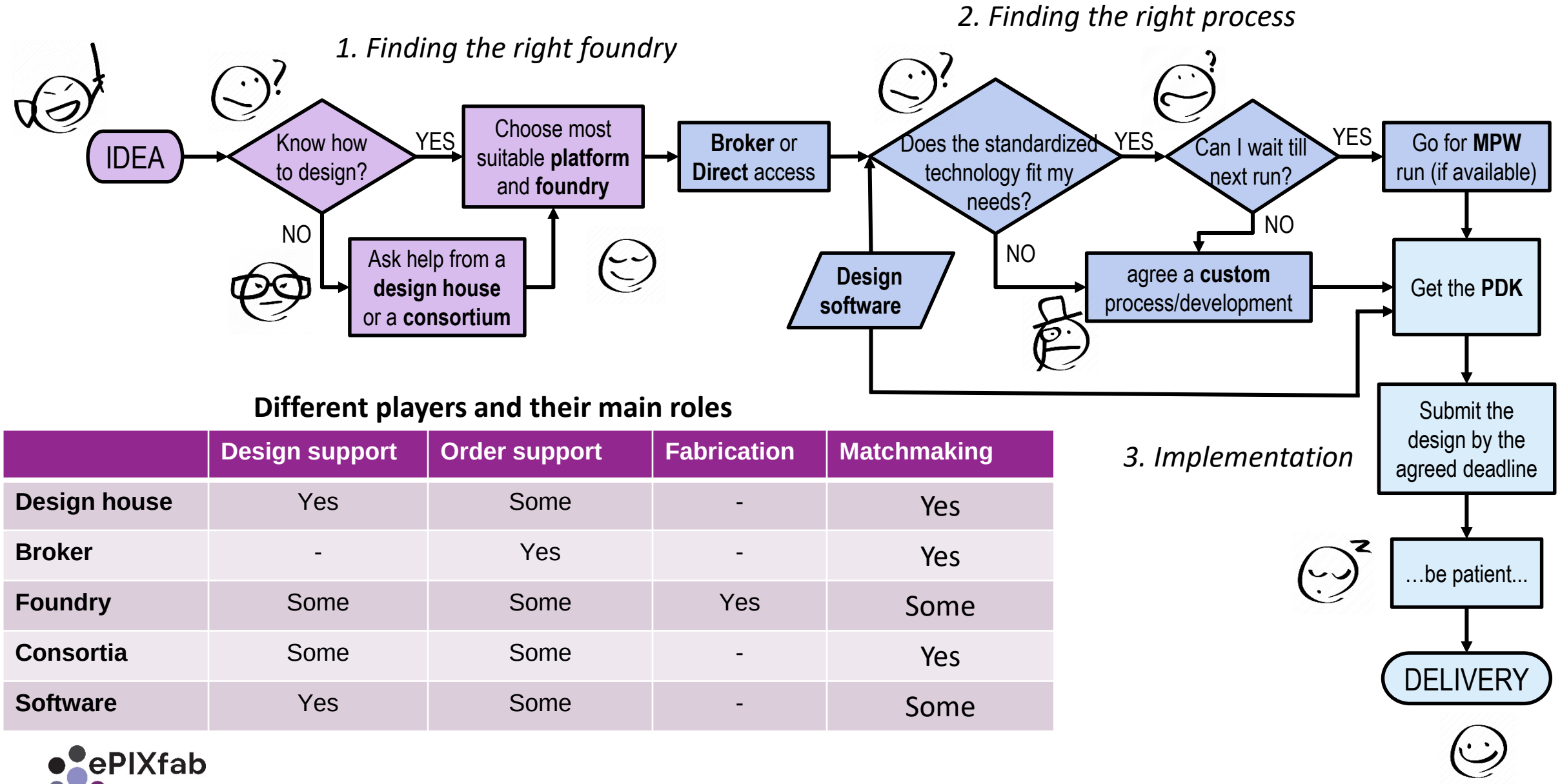
Evolution of silicon photonics prototyping & manufacturing



Economy of (wafer) scale for a standardized platform



Open access workflow: various ways to go



Different players and their main roles

	Design support	Order support	Fabrication	Matchmaking
Design house	Yes	Some	-	Yes
Broker	-	Yes	-	Yes
Foundry	Some	Some	Yes	Some
Consortia	Some	Some	-	Yes
Software	Yes	Some	-	Some

With permission from: Matteo Cherchi (VTT)

ePIXfab Members

ePIXfab Members

Silicon photonics platforms

Thin SOI (< 1 µm)

- ✓ Compact components
- ✓ High speed active devices
- ✓ High efficiency grating based fibre couplers
- ✓ Telecoms applications
- — Two photon absorption (TPA)
- — Higher propagation losses

Thick SOI (> 1 µm)

- ✓ Low-loss components
- ✓ High power applications
- ✓ Mid-IR applications
- ✓ Polarisation independence
- — Low speed active components
- — Large bend radius

Silicon nitride

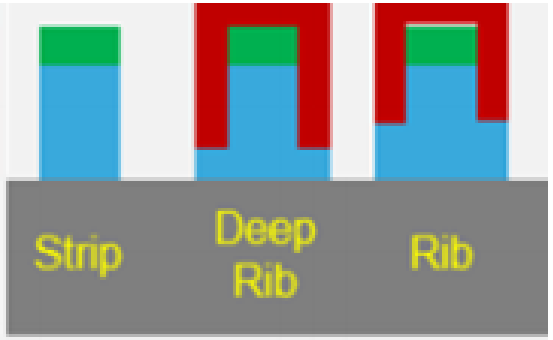
- ✓ Very low propagation loss
- ✓ Visible wavelength applications
- ✓ High power applications (no TPA)
- ✓ Low temperature sensitivity
- — No active components
- — Large component footprint

Ge-on-Si

- ✓ Low-loss components
- ✓ Mid-IR applications for sensing etc.
- ✓ Free-space communications
- — Lower speed active components
- — Larger components

*Example open-access foundries – not intended to be exhaustive

ST Microelectronics Silicon Photonics Platform: Bilateral Mode

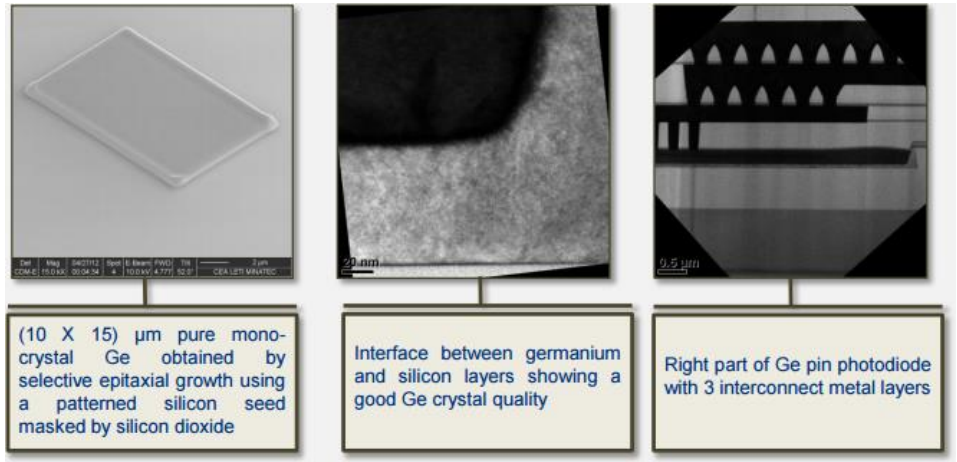


WG Loss

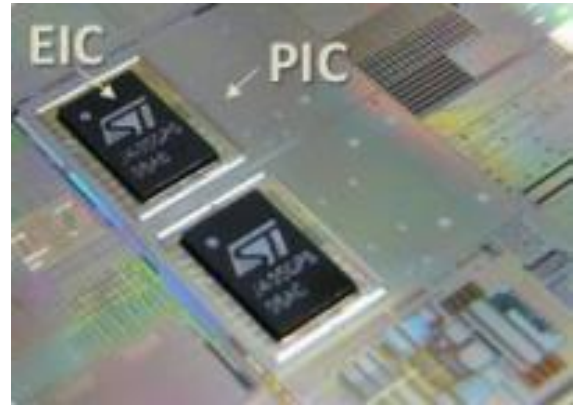
350nm strip: IL: 3.5 dB/cm

320nm deep-rib: IL: 3.7 dB/cm

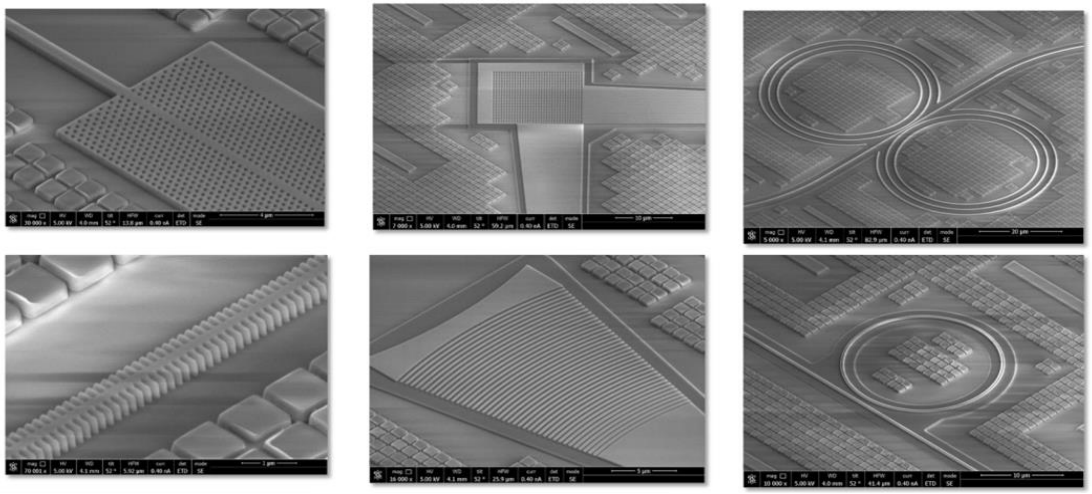
400nm mid-rib: IL: 1.4 dB/cm

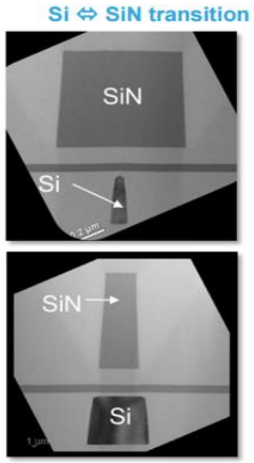


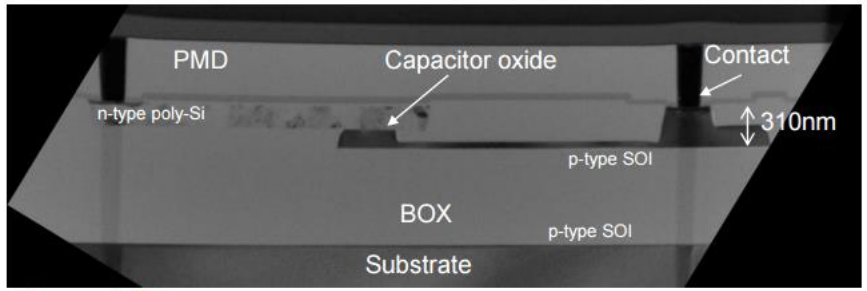
Germanium Integration for High Speed Photodetector



System Integration:
3D integration of EIC & PIC







Loss < 9dB/mm
Phase Shift ~ 40°/mm @ 1.8V

Capacitive Si-MOS Modulator

Integrated Silicon Nitride

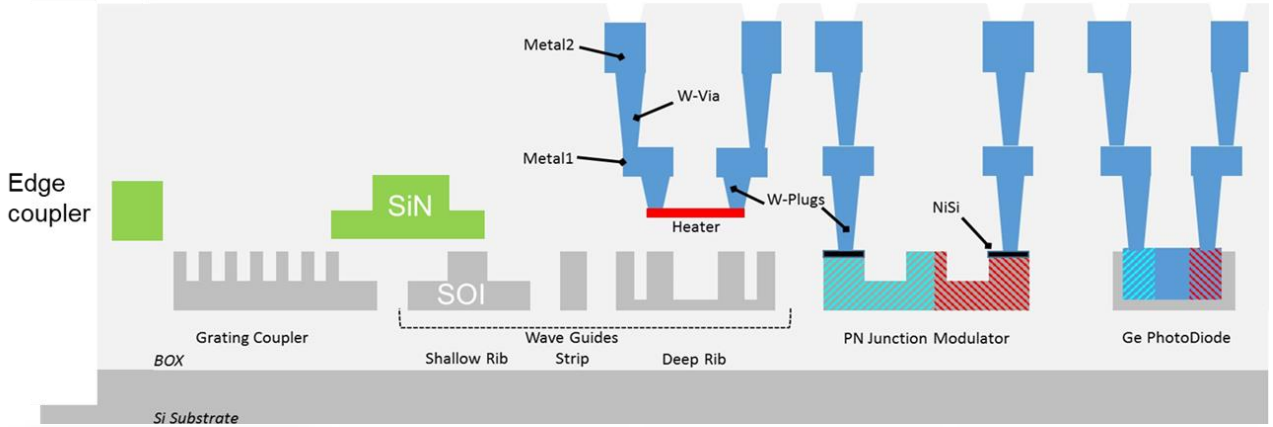
Passives: 1D & 2D Strip Photonic Crystals, 1D & 2D Rib Grating Couplers,Deep-Rib Ring Resonators

High-volume Manufacturing **Beyond 100 K chips or 100 wafers**

CEA-leti's platform: Dedicated Engineering Runs

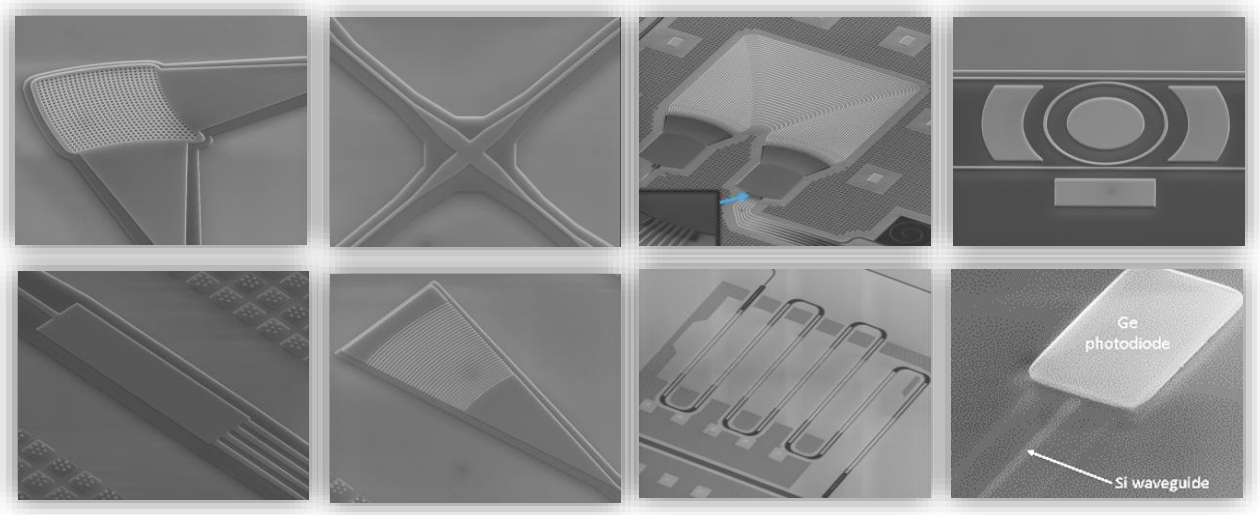
Advanced 300mm Si platform

- Design, Process integration, Test
- 220nm and 310nm SOI with 3 etch levels, metal heater and planarized BEOL with 2 routing levels
- 60nm smallest feature size



Versatile

- Comprehensive library of mature O/C-bands components
- PECVD SiN layer option
- III-V on Si by direct bonding (wafer or dies) for lasers
- Grayscale lithography for mirror integration

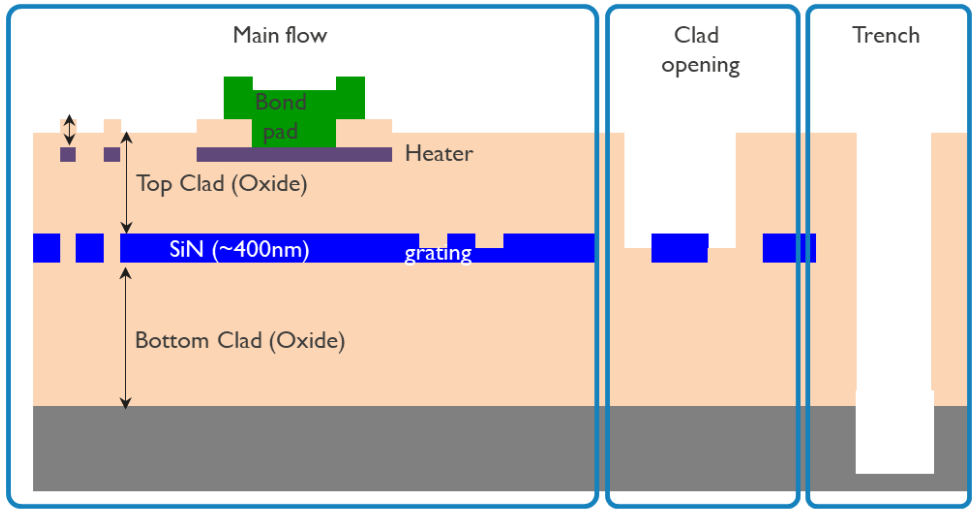


Low optical losses

- Si waveguides: 0.1-1.1 dB/cm (rib/strip)
- PECVD SiN waveguides: 0.6 dB/cm

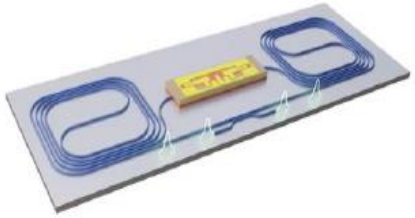
Low-volume Manufacturing — **Up to 100 K chips or 100 wafers**

Imec SiN platform: Dedicated Engineering Mode

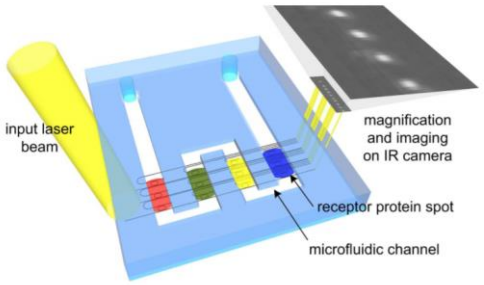


https://www.imec-int.com/en/what-we-offer/development/system-development-technologies/Integrated-photonics/silicon-nitride-based-photonics

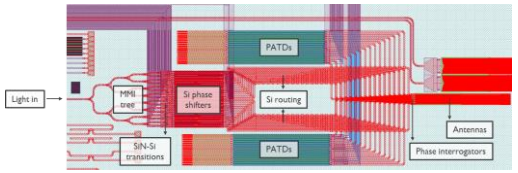
- Extreme thickness control (<1 nm)
- Low propagation loss from 400-2200 nm
- Small bend radii (small footprint)
- High power handling
- Processing on Si & quartz wafer
- Low coupling loss (GC and EC)
- Integration with SiP advance actives (modulator, GePD)
- Wafer bonding capability (e.g. CMOS wafer to photonic wafer)



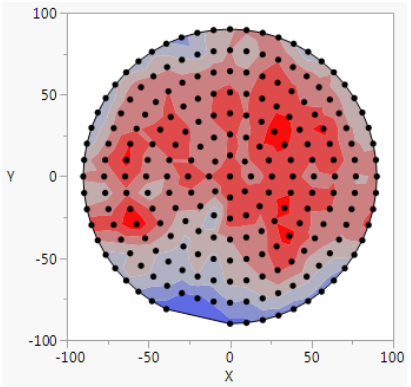
Advance laser

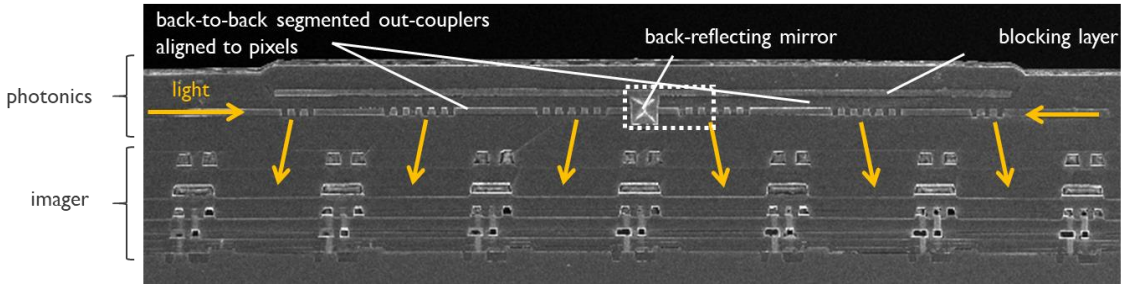


Life Science



Lidar





Low-volume Manufacturing **Up to 100 K chips or 100 wafers**

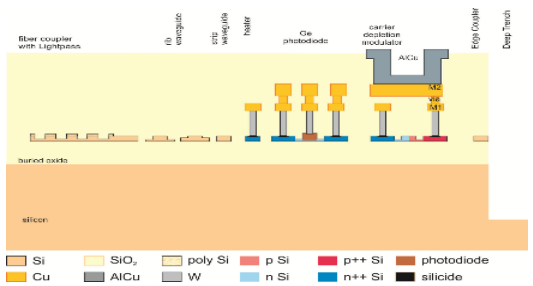
Standardized Open Access SOI Technologies via MPW through brokers

Accessible through MPW and dedicated engineering runs

imec

PSV+

ISIPP50G



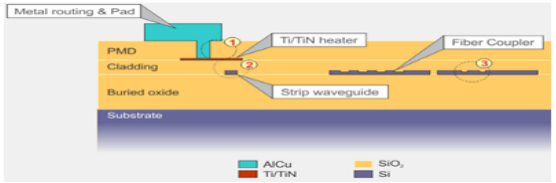
220 nm SOI platform

O and C band

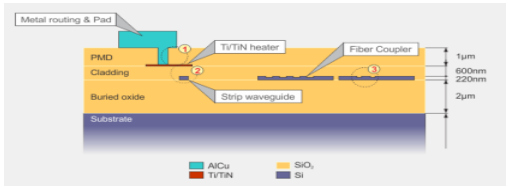
50G active devices

leti

Passive + heaters



Si310-PH



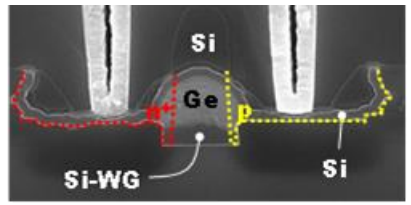
310, 220 nm SOI platform

O band devices compatible

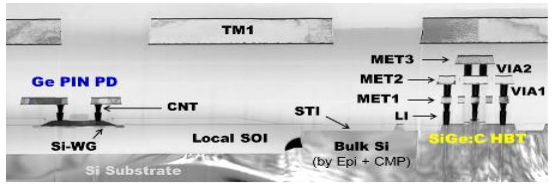
for III-V laser integration

ihp

IHP SG25_PIC



IHP SG25H4_EPIC



Photonic BiCMOS

Monolithic integration C-band

& BiCMOS (190GHz HBT)

EUROPRACTICE IC SERVICE

cmp

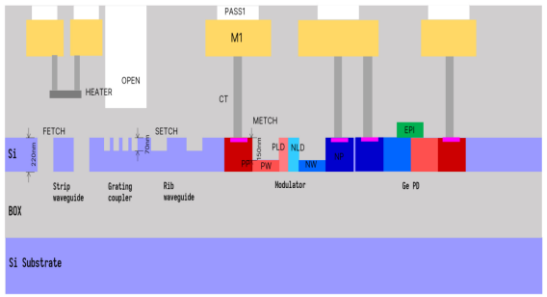
Low-volume Manufacturing — **Up to 100 K chips or 100 wafers**

Standardized Open Access SOI Technologies via MPW (Direct Access)

Accessible through MPW and dedicated engineering runs

UMEC 联合微电子中心

CSIP180AI

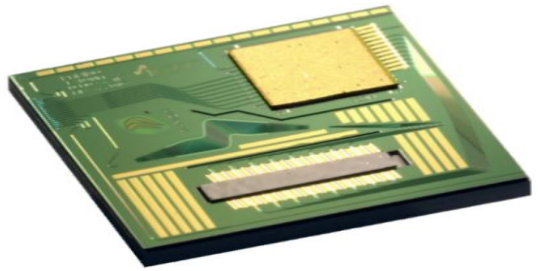


220 nm SOI platform

50Gb/s device library

VTT

Passives
+ Implanted heaters
+ Implanted PIN
+ Flip-chip



Thick SOI

low loss + pol. independent

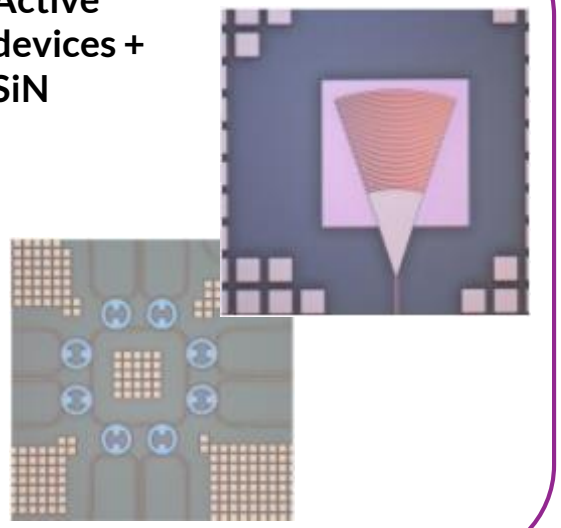
Low-volume Manufacturing **Up to 100 K chips or 100 wafers**

Standardized Open Access SOI Technologies: Rapid Prototyping

Rapid Prototyping and Customized Prototyping Services

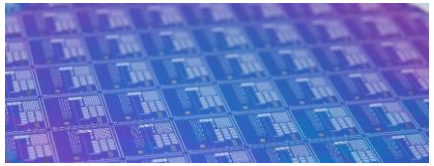
Fondazione INPHOTEC

Active devices + SiN

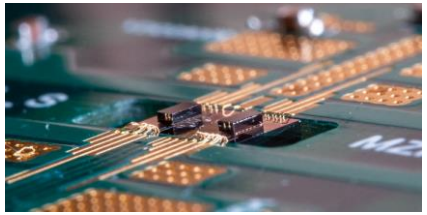


CORNERSTONE

Open-source access to multiple platforms for emerging applications



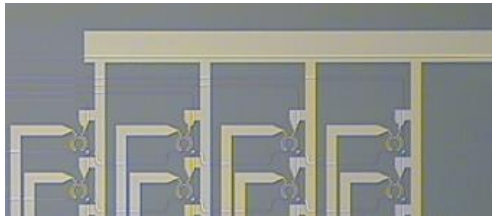
Electronic-photonic integration

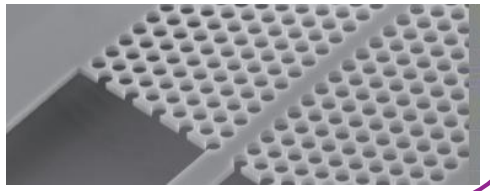


UNIVERSITY OF Southampton

AMO

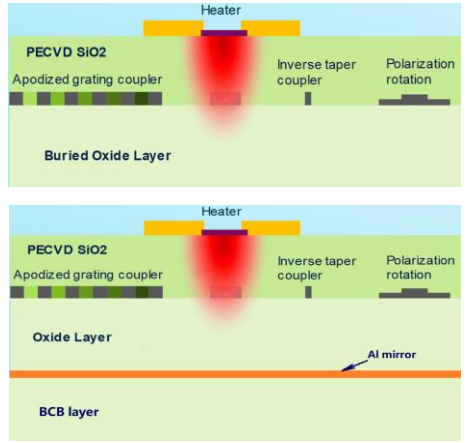
Actives + Passives on 220nm and 340 nm SOI using e-beam & projection lithography





SiPhotonIC TECHNOLOGIES

Actives+Passives on 220nm And 340 nm SOI using e-beam



220 nm SOI platform

E-beam lithography

Hybrid DUV + e-beam litho

220,340,500nm SOI, SiN, Ge-on-Si, suspended-Si platforms

Flexible foundry platform

for customized wafer runs

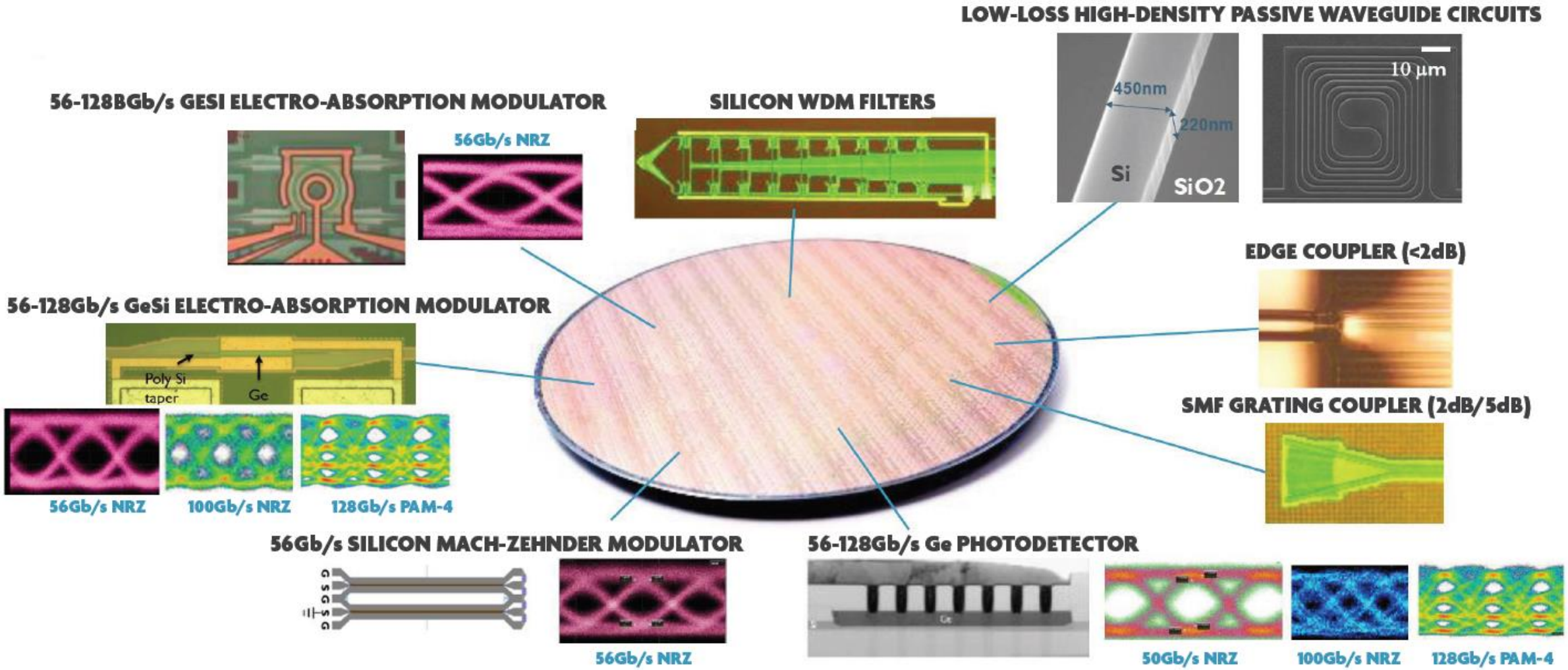
250 nm SOI platform

Platforms with and without Al Mirrors

Prototyping/MPW **Up to 1 K chips or 1 wafer**

Technology Updates 2021

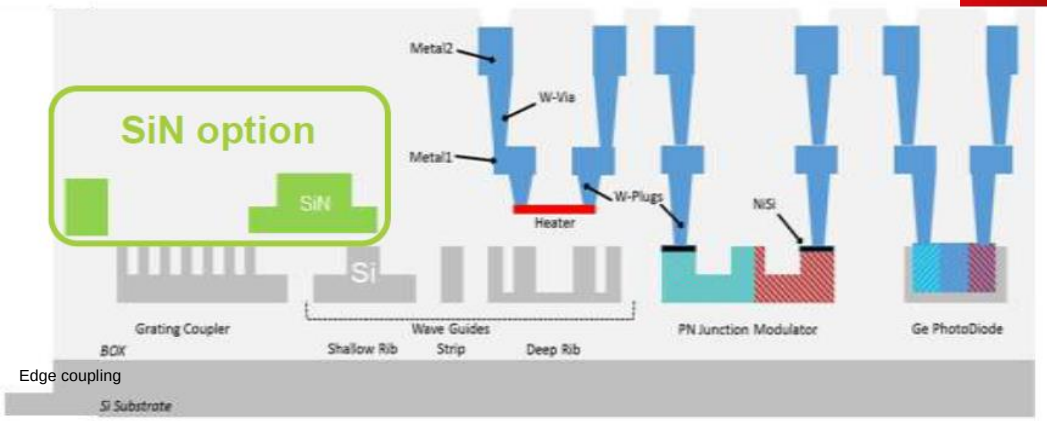
imec's iSiPP50G platform



CEA-LETI Si-310 technology

Process characteristics → state-of-the art technology

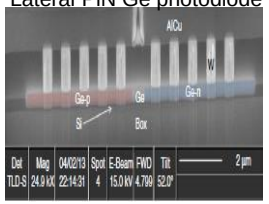
- 310nm SOI & 2µm BOX on 300mm wafers
- Ge deposition for photodiodes and SiN module option
- 193nm immersion lithography enabling feature size down to 100nm
- 3 Si patterning steps for waveguides & 6 implant operations for modulators
- 2 metal layers for optimal routing & bump deposition for flip-chip

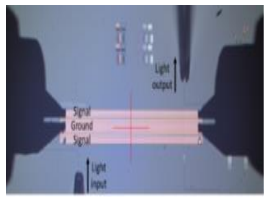


Cross-sectional schematic

Library contents & indicative performances → high performance building blocks for 1310 & 1550nm

Lateral PiN Ge photodiode





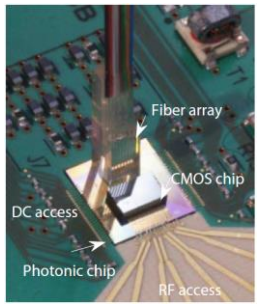
Mach-Zehnder modulator

Active components	Specifications	Value @ 1550nm
Mach-Zehnder modulator	OE bandwidth @ -4V	40GHz
	Vpi.Lpi @ -2V	< 2V.cm
Ring racetrack modulator	OE bandwidth @ -2V	> 15GHz
	Vpi.Lpi @ -2V	< 2.5V.cm
Longitudinal PiN Ge photodiode	EO bandwidth @ -1V	> 35 GHz
	Dark Current @-1V	< 55nA

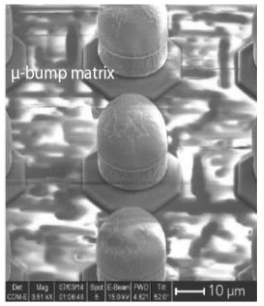
Passive components	Specifications	Value @ 1550nm
Strip, rib & deep rib waveguides	Loss	< 1dB/cm
Transitions	Loss	< 0.03dB
1D grating coupler	Insertion loss	< 2.5dB
2D grating coupler	Insertion loss	< 3.5dB
Ring filter	Quality factor	> 10,000
MultiMode interferometer 1x2	Loss	< 0.2 dB

Applications → well-adapted to R&D

- Comunication: telecom/datacom, 5G infrastructures
- Computing: quantum & neuromorphic computing
- Optical sensing: gas sensing, health monitoring…



3D system integration



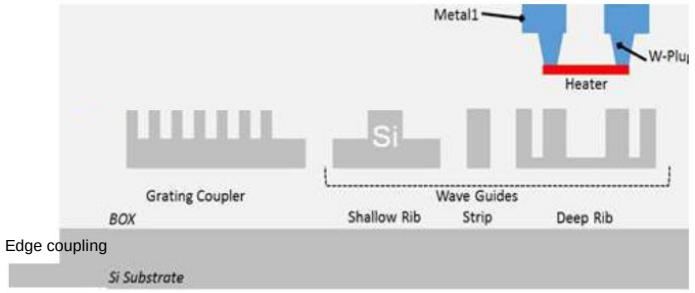
Bump deposition

MPW offer

- 1 run offered per year
- Price based on circuit area
- PDK available with Cadence, Tanner & Synopsys tools

CEA-LETI Si-220 & Si_3N_4-800 technologies

Si-220



Cross-sectional schematic

Process characteristics

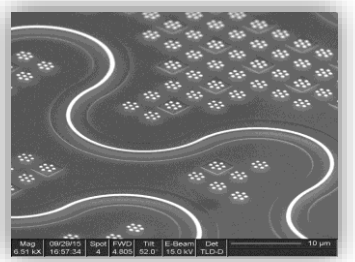
- 220nm SOI & 2µm BOX
- 300mm wafers
- 193nm immersion lithography
- Passive components only

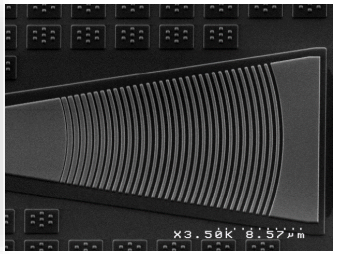
- 800nm LPCVD Si3N4
- 200mm wafers
- 200nm CDmin
- Passive components only

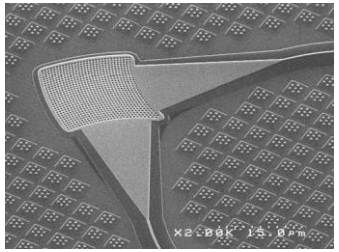
Si_3N_4-800

Cross-sectional schematic

Library contents & indicative performances


Highly-confined waveguides


1D grating coupler


2D grating coupler


Heaters

Components	Specifications	Value @ 1550nm
Straight & bend waveguides	Loss	Down to 0.03 dB/cm
1D grating coupler	Insertion loss	< 12.5 dB
MultiMode Interferometer 1x2	Insertion loss	< 0.1 dB
MultiMode Interferometer 2x2	Insertion loss	< 0.5 dB
Racetrack resonators	Attenuation coefficient	3 dB/m
	Quality factor	10^7

+ transitions (singlemode to multimode), directional couplers, multimode interferometers…
Performances close to those obtained with Si-310 technology

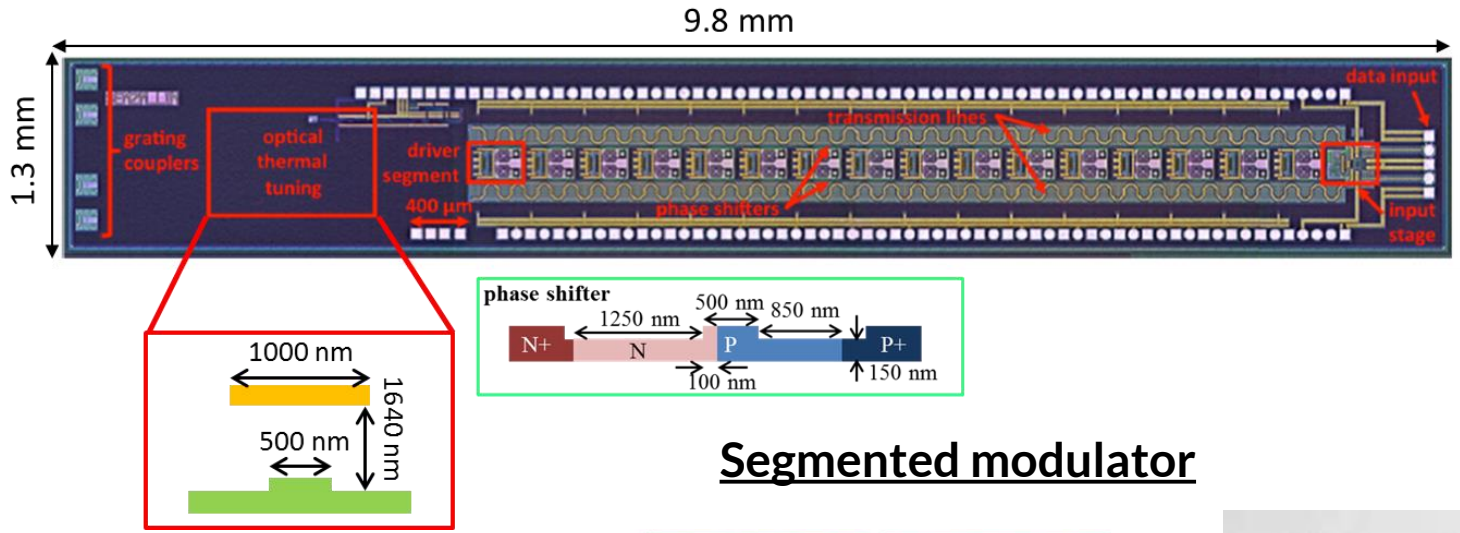
Applications

- Comunication, computing & optical sensing for Si-220
- Optical sensing, non-linear optics and quantum photonics for Si_3N_4

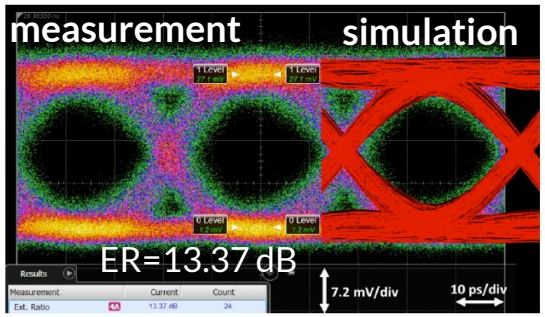
MPW offer

- 1 run offered per year for Si-220/1 or 2 for Si_3N_4
- Price based on circuit area
- PDK available with Cadence tool

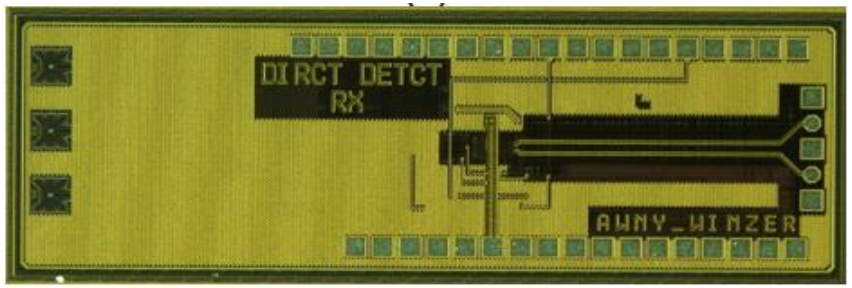
IHP's photonic-electronic platform



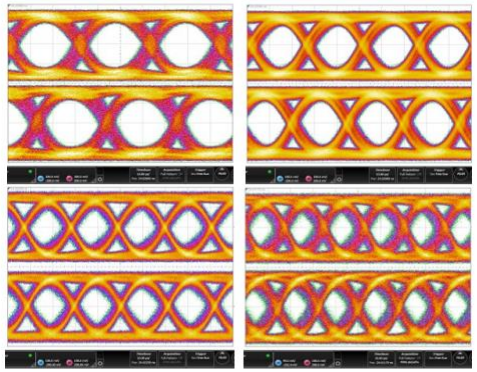
28 Gb /s

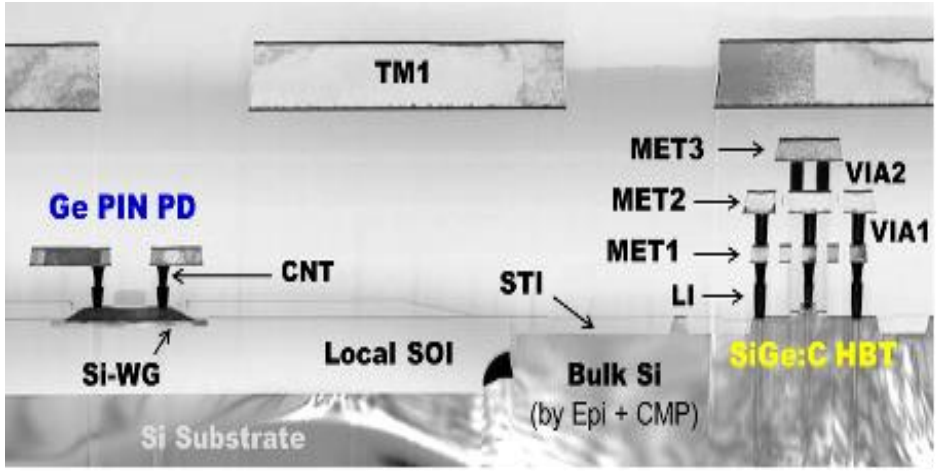


Segmented modulator



Receiver up to 56Gbps





VTT Thick Silicon Photonics Platform

Main features

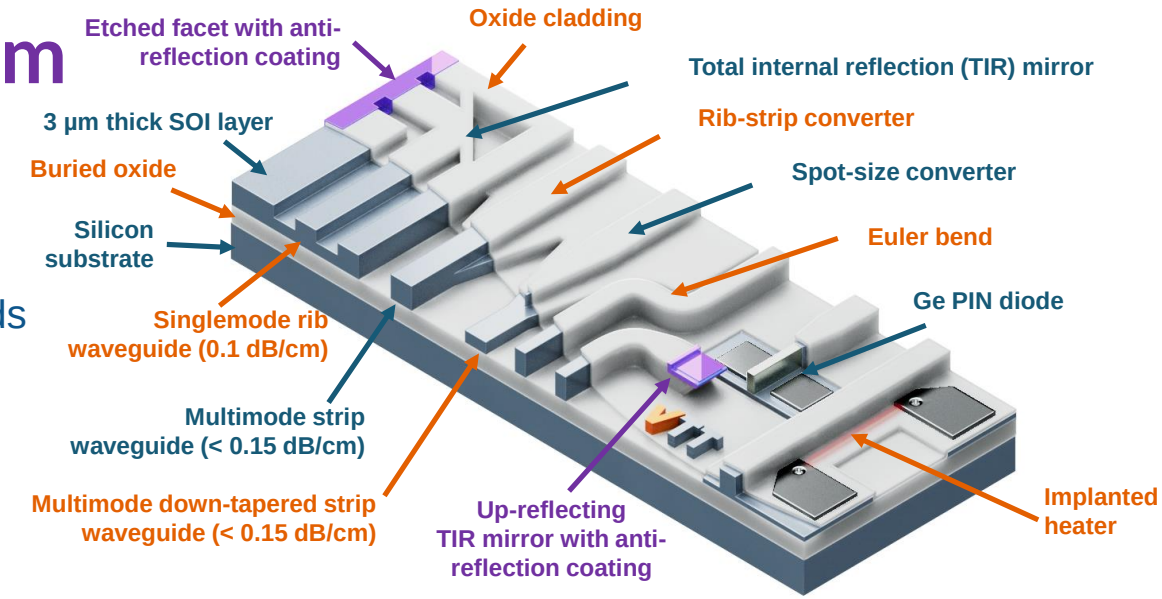
- Micron-scale thick SOI technology based on UV stepper[1]
- Hybrid integration of III-V chips (lasers, SOAs, EAMs…)
- Unique combination of low-loss (0.04 - 0.15 dB/cm) and small bends
- Ultra-broadband operation (1.2 to 4 µm and beyond)
- High power handling (≈ 1 W)
- Small polarization dependency

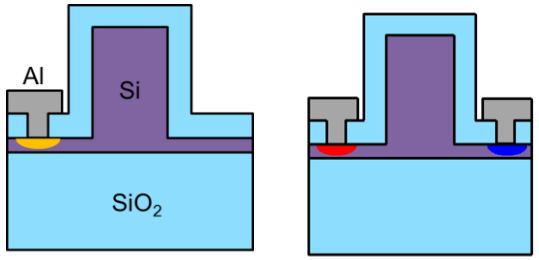
Applications

- Telecom/Datacom
- Sensing and spectroscopy
- Imaging (OCT, LIDAR)

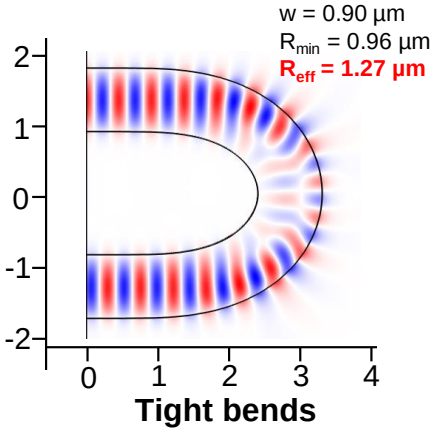
Achievements

- Low-loss low-cross-talk (de)multiplexers[1]
- Proprietary micron-scale bends[2]
- Compact and low-loss spiral waveguides[3]
- Up to 8 million Q ring resonators[4]
- Monolithic integration of fast (>40GHz) Ge PDs[5]
- Zero-birefringence strip waveguides[6]

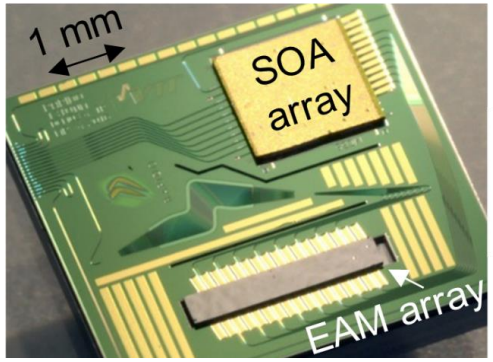




Phase shifters, either based on Implanted heaters or PIN junctions



Tight bends



Hybrid integration of III-V on Si

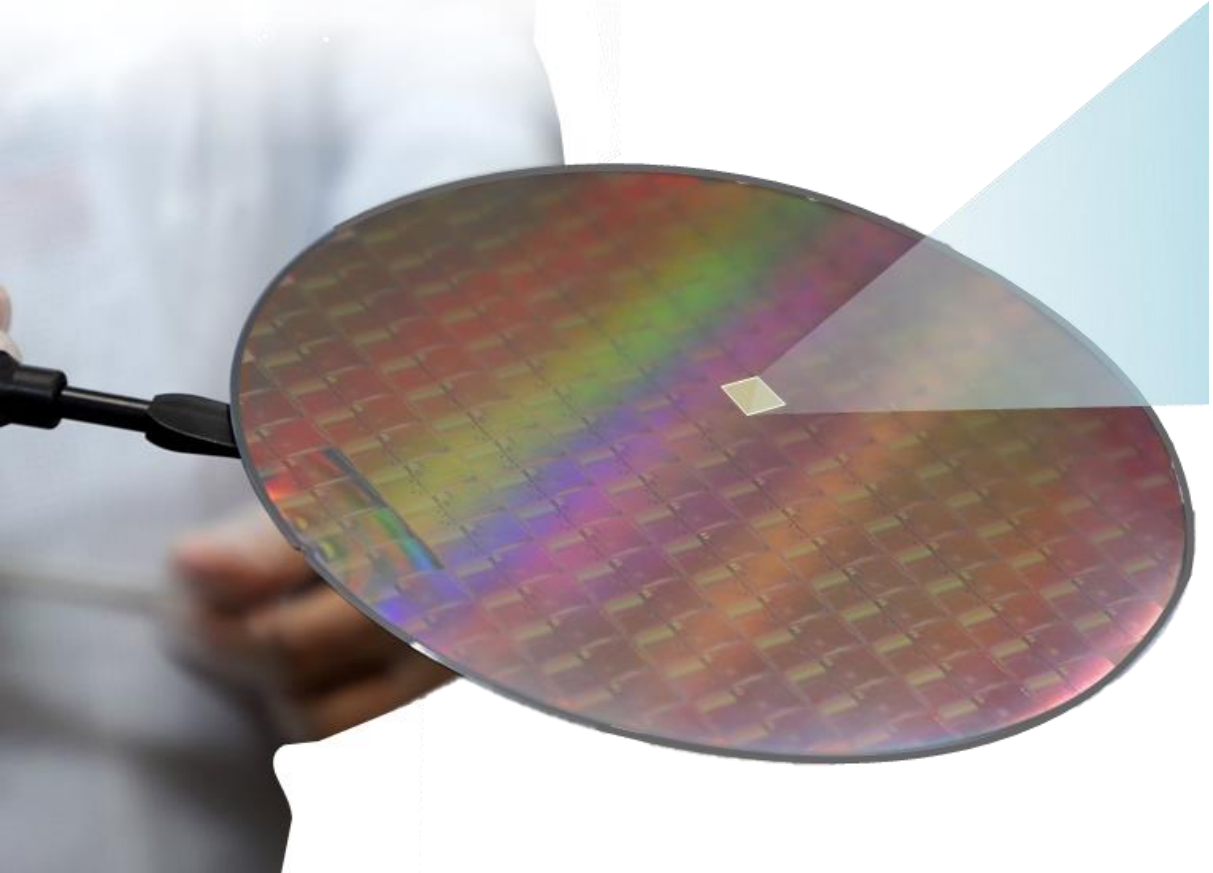
[1] https://doi.org/10.1109/JSTQE.2019.2908551
[2] https://doi.org/10.1364/OE.21.017814
[3] https://doi.org/10.1364/OPTICA.2.000751
[4] https://doi.org/10.1364/OL.395203
[5] https://doi.org/10.1117/12.2542165
[6] Timo Aalto, invited at ECOC 2017

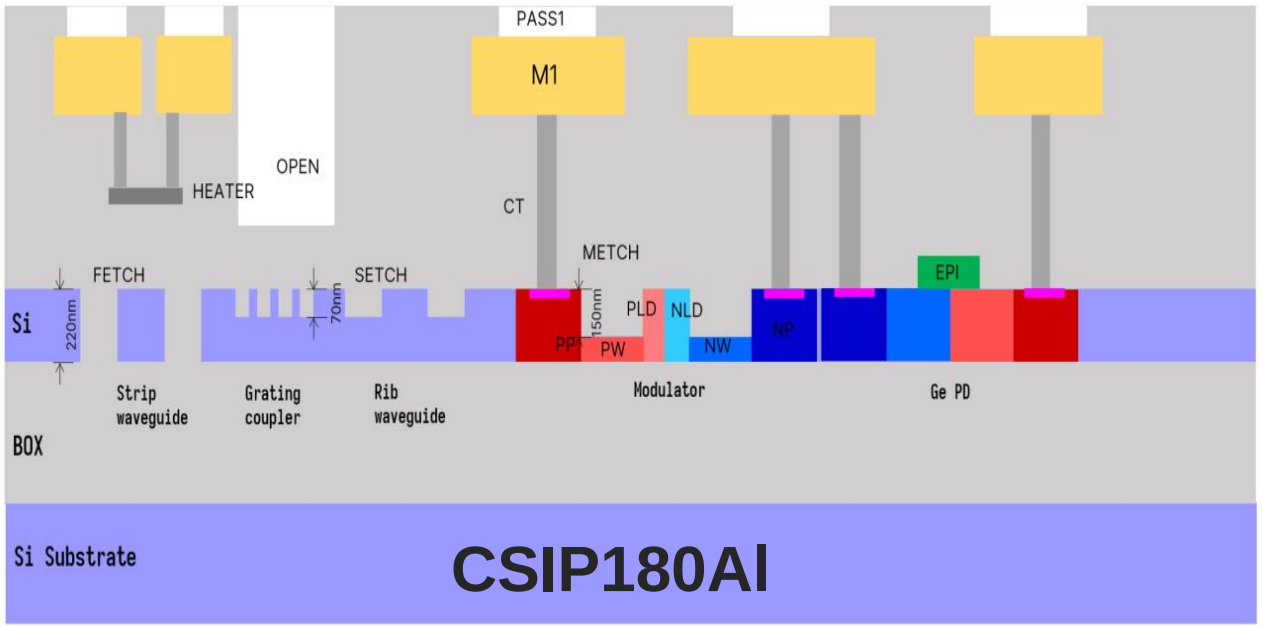
Open access platform[1]
through biannual **MPW runs** (PDK available)
silicon.photonics@vtt.fi

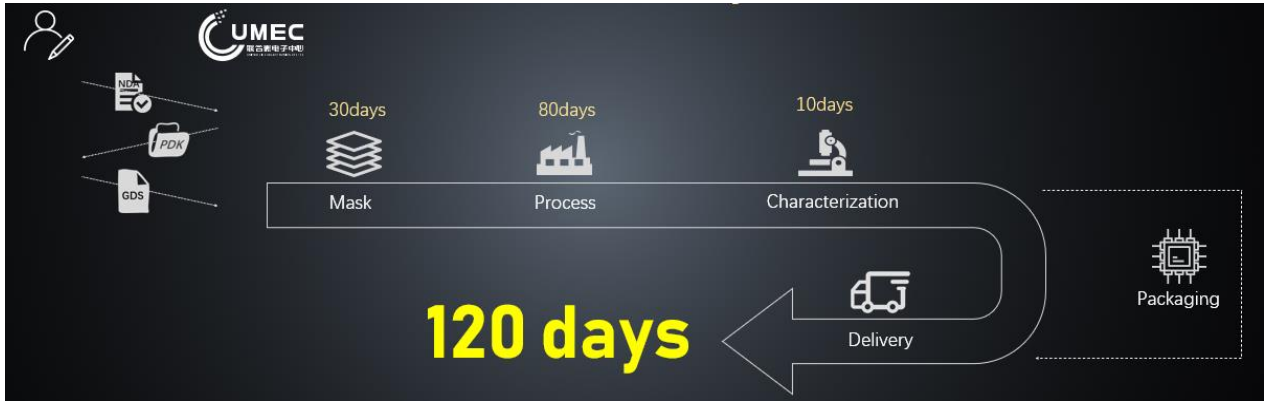
Silicon Photonics Platform

Ref: https://service.cumec.cn/

- 180nm technology node (130nm in 2021)
- Passive & Active devices
- >50Gbps device library…





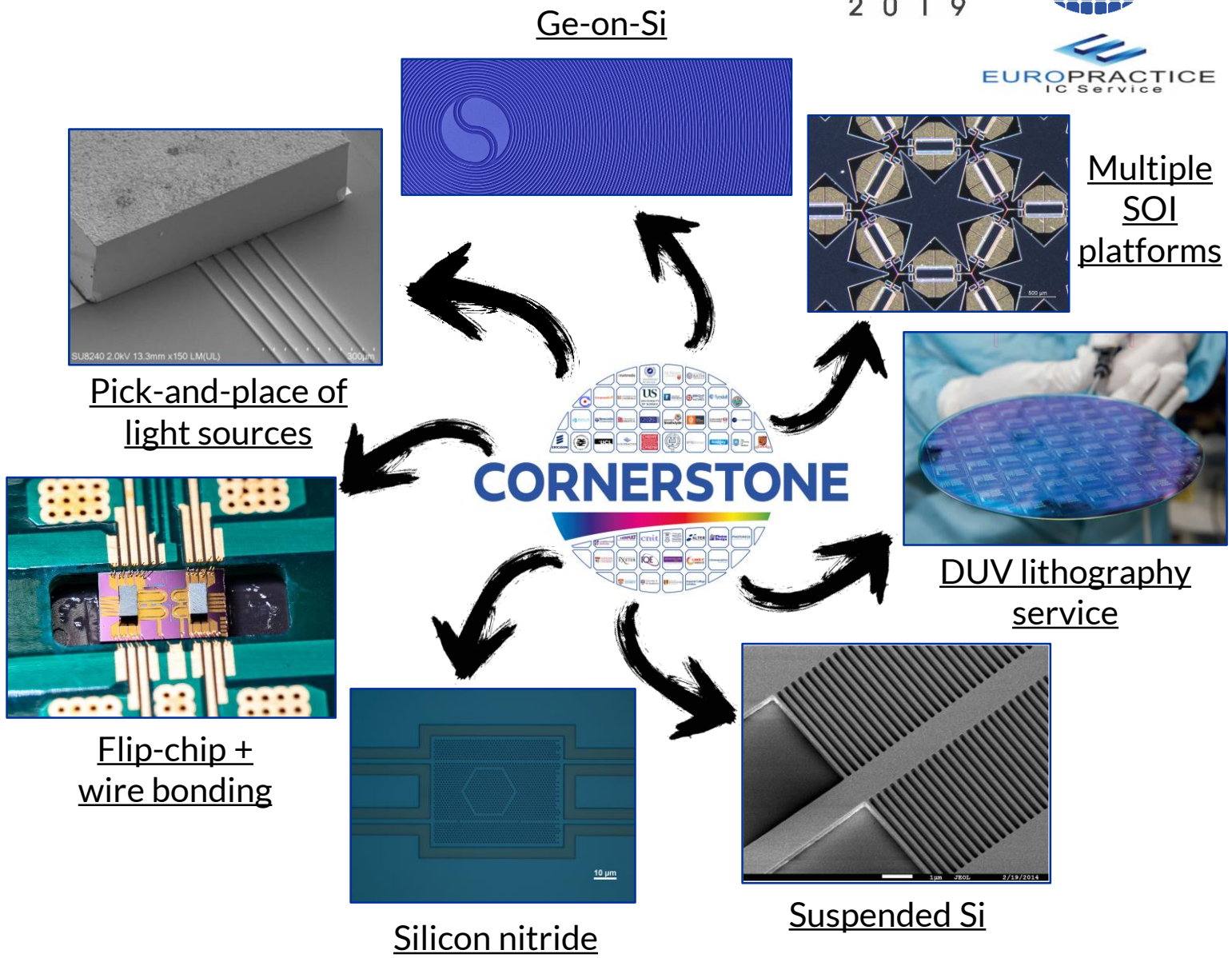


CORNERSTONE's flexible rapid prototyping platform

- License free, open-source platforms
- Hybrid DUV + e-beam lithography to enable seamless scaling to higher volumes
- Multiple platforms for visible, telecom and mid-IR wavelengths
- Versatile fabrication processes via MPW service & bespoke batches
- Design consultancy available

Core values:

- To give process flexibility back to the designer
- To enable rapid prototyping using scalable technology

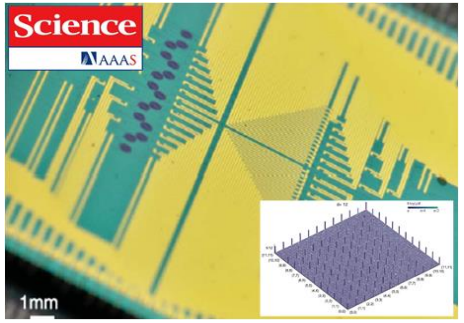


SiPhotonIC's platform

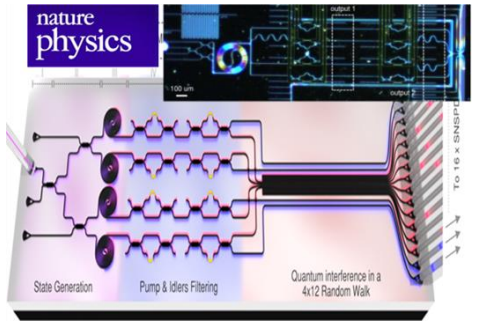
- State-of-the-art 100kV E-Beam Writer JBX-9500FSZ
- Advanced SOI platform
  - Al mirror introduced with grating coupler for ultra-low loss fiber-to-chip coupling
  - Efficient Ti metal heater
  - Full building blocks to build your silicon PICs
  - Large scale silicon PIC prototyping
  - Ultra-small structure resolving
  - Fast turn over period

Typical components	Performances
Grating coupler	coupling loss: <1.0 dB
Strip waveguide	Propagation loss: <2.5dB/cm
Mach–Zehnder switch	Insertion loss: <0.1dB
Cross intersection	Insertion loss:~0.1dB/cross Crosstalk: <-40dB
Thermal tunable phase shifter	Tunability: > 2π

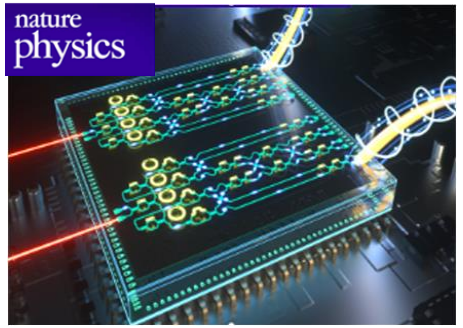
- Selected publications



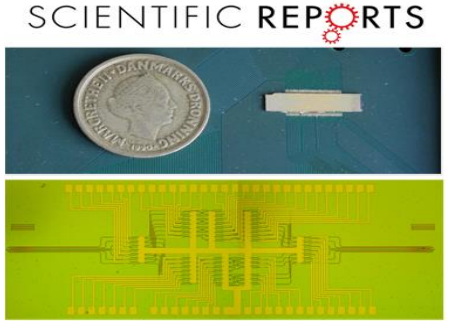
- Large-scale silicon quantum chip for high-dimensional quantum entanglement generation and manipulation.



- Silicon quantum photonic chip for generation and sampling of quantum states on chip.



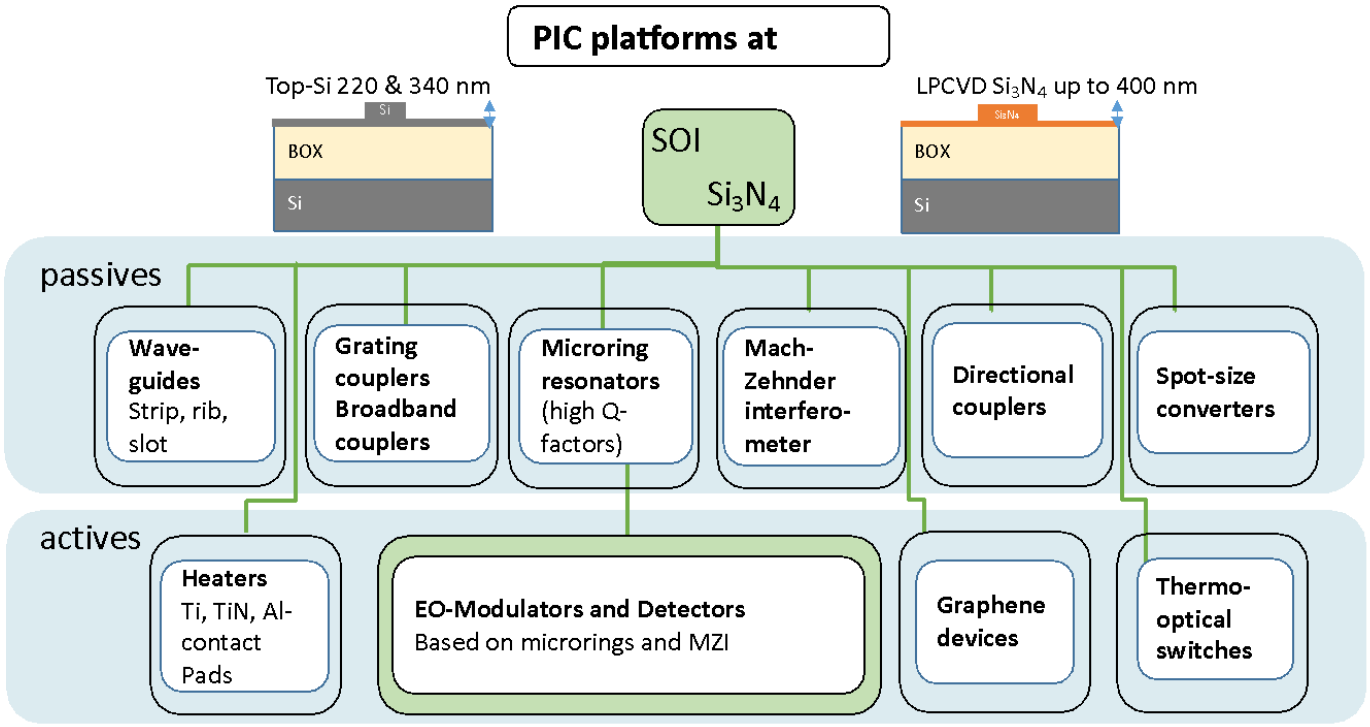
- Silicon quantum photonic chip for quantum teleportation and multiphoton entanglement.

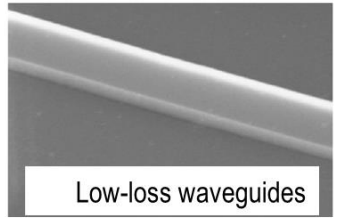


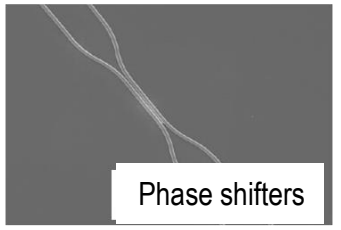
- Silicon chip for multicore fiber switching.

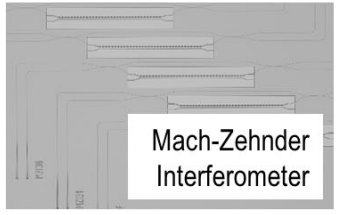
AMO's eBeam-based prototyping of SOI and silicon nitride PICs

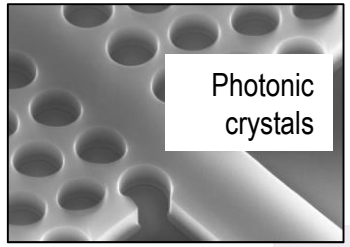
Customized SOI R&D services	
SOI	**Si_3N_4**
150 mm SOI with 220 nm Si on 3 µm BOX	150 mm Si wafers with thermal oxide (2.3 µm or 6 µm) with 100-400 nm LPCVD Si_3N_4
Mix&Match Lithography resolution: electron beam (< 100 nm) and i-line stepper (500 nm)	
3 (Full, shallow, deep waveguides) etch levels	2 etch levels; Ultra low loss cladding options
Vias, implantation steps up on request	
2 layer metallization	











Available on Si_3N_4 and SOI platform

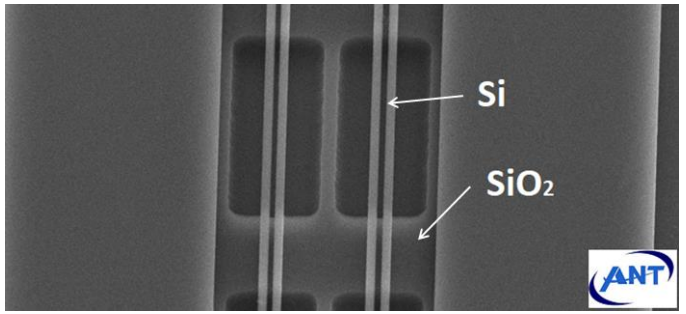
Only available on SOI platform

→ **Flexible foundry platform for customized wafer runs with short turnaround times**

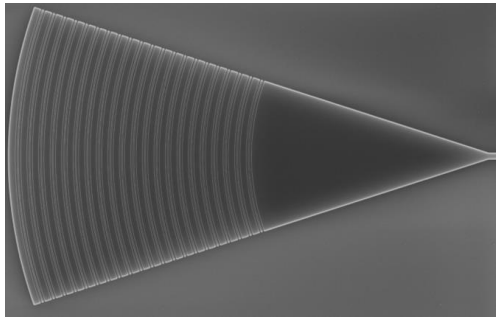
→ **Ultrafast prototyping**

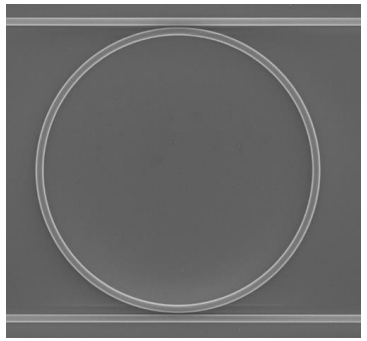
Applied Nanotools e-beam prototyping platform

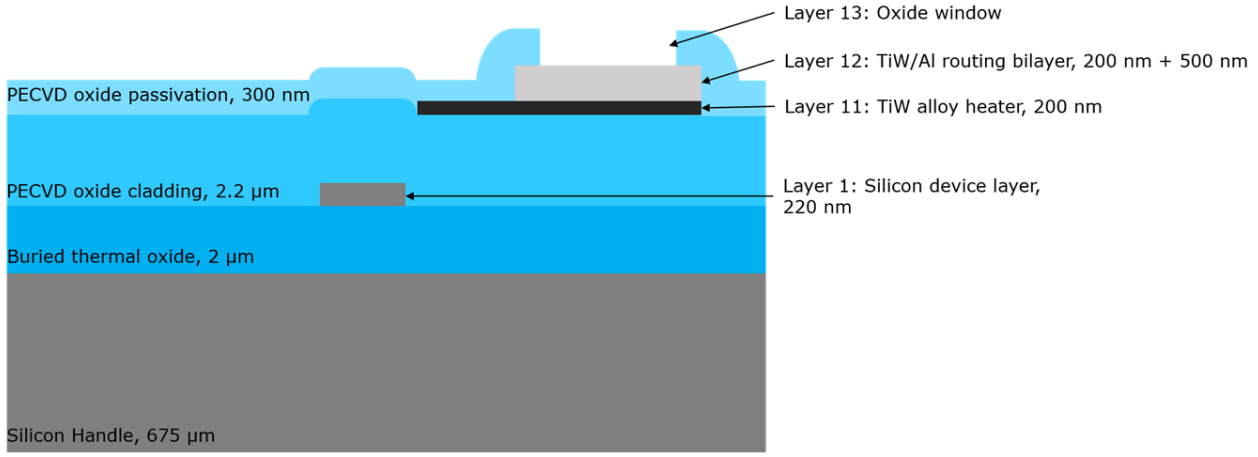
- Various platforms available: 220 nm, 300 nm, 500 nm SOI and 400 nm SiN
- 70 nm minimum feature size (suitable for sub-wavelength devices)
- Fast turnaround time and competitive pricing
- Efficient TiW metal heaters for >2π phase shifting
- Low-loss waveguides with < 2 dB/cm propagation loss
- Vertical grating couplers and edge couplers available in our PDK
- Online resources, submission system and design rule checks via. Design Center: https://www.appliednt.com/nanosoi/sys/
- 8 multi-project wafer (MPW) runs provided annually; dedicated runs available by request
- Custom fabrication options: multi-layer etching, custom metal, oxide window openings, suspended waveguide devices, etc.



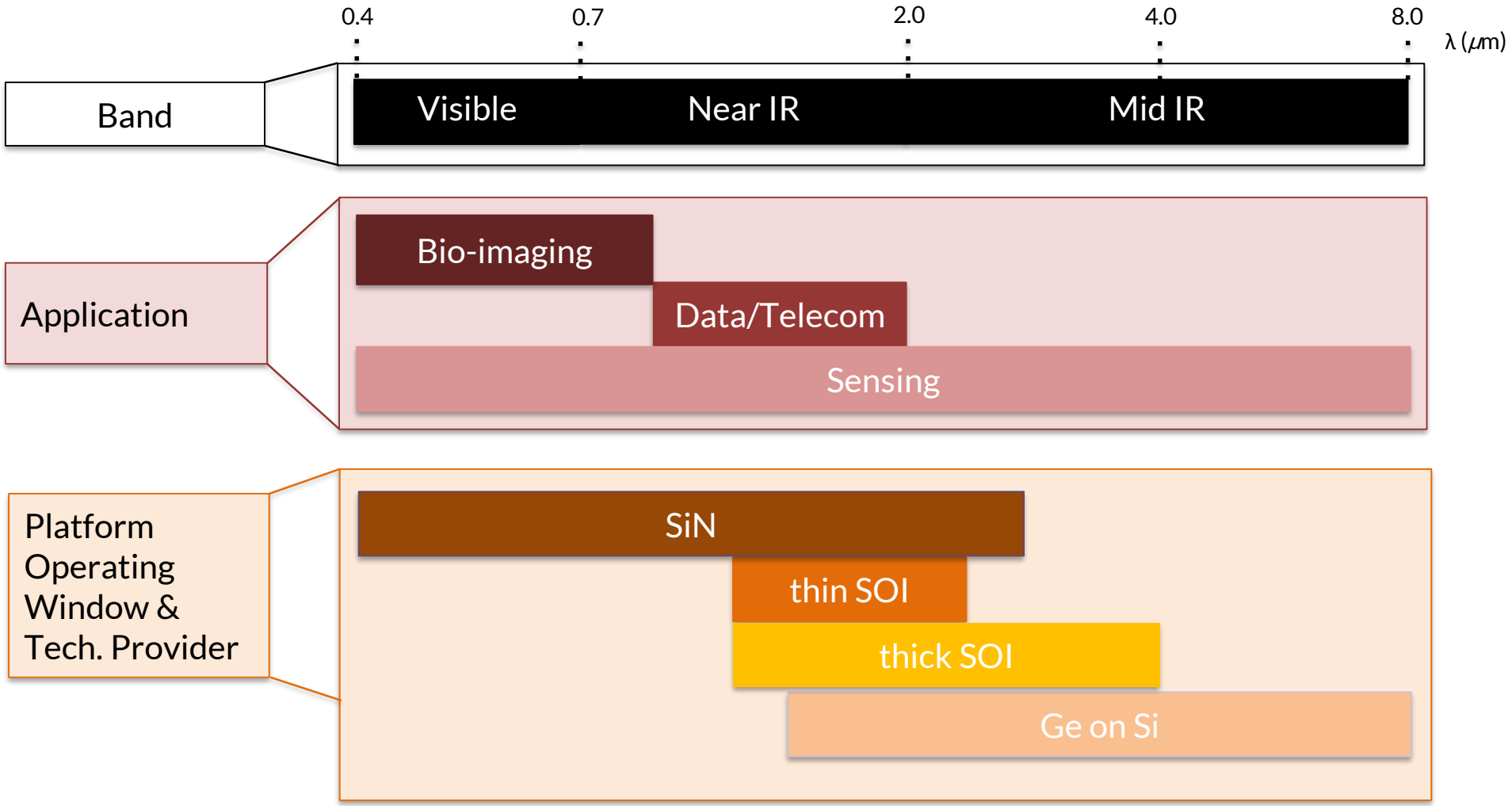
Suspended slot waveguides


Vertical grating coupler


Microring resonator



Expanding silicon photonics portfolio



The European Silicon Photonics Alliance

Limitations of current silicon-on-insulator PICs*

Spectral transparency: shortest λ	1.1 µm	Silicon bandgap
Spectral transparency: longest λ	4 µm	SiO2 absorption
Optical power limitation (1.3/1.5µm)	10's of mW	Two-photon absorption
Distributed backscatter	%'s per cm	nm-level sidewall roughness + HIC
Optical pathlength error	0.1% - level	nm-level width inaccuracy + HIC
T-sensitivity of pathlength	0.01%/K	Thermo-optic coeff. silicon
Layer stack flexibility	Limited	SOI-wafers made by bonding
Integration with CMOS electronics	Challenging	Technical or economic mismatch
Source integration	Challenging	Technology not available in CMOS-fab

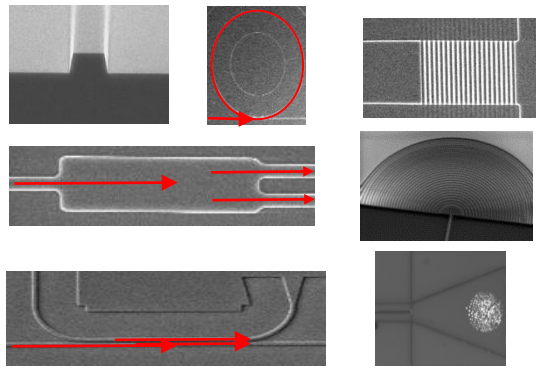
Silicon Photonics beyond Silicon

* The limitations are mostly relevant for thin SOI

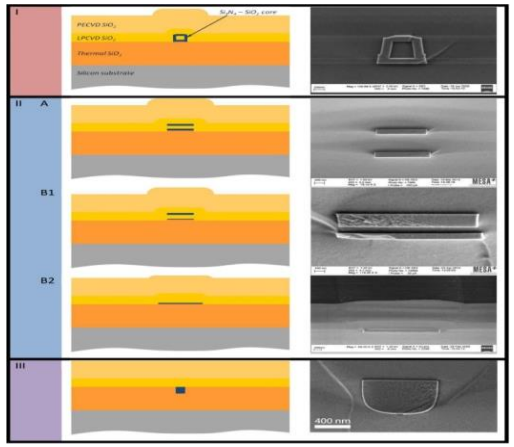
Open Access Silicon Nitride Technologies

Accessible through MPW (via brokers or directly) and dedicated engineering runs

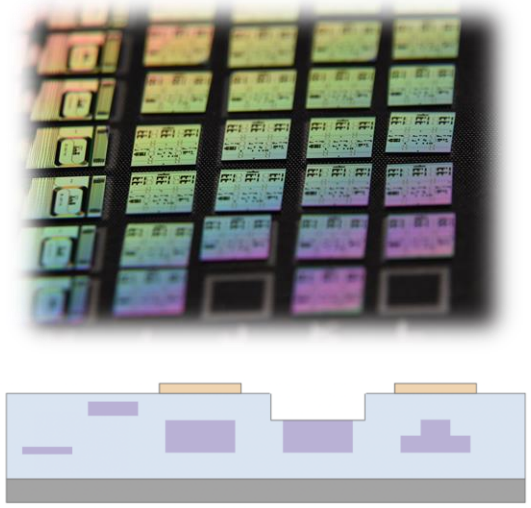
imec



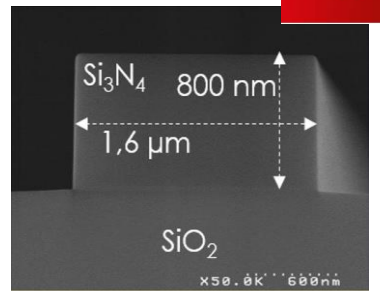
LioniX International

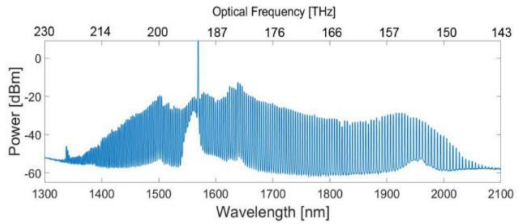


LIGENTEC



leti





BioPIX PECVD SiN platform

High performance platform for life-science applications at visible wavelength ranges

TriPleX™: *Ultra low loss building blocks for telecom, bio photonics and bio sensing applications*

LPCVD SiN (100nm-850nm)

SiN core for low loss visible, telecom and MidIR

LPCVD SiN (250nm, 300nm and 800nm thick)

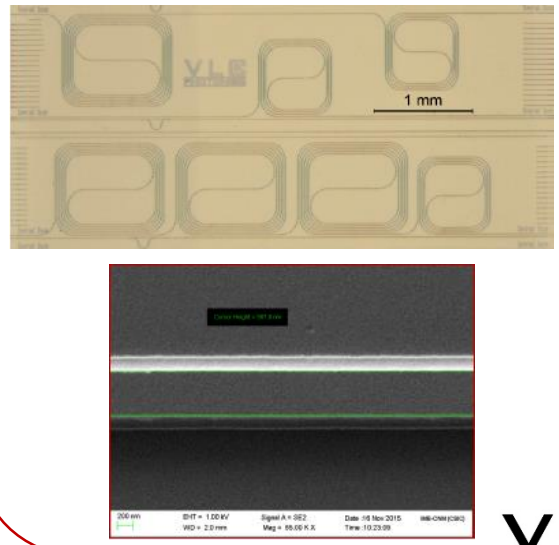
Biosensors, Quantum photonics, Non-linear optics

Low-volume Manufacturing **Up to 100 K chips or 100 wafers**

Open Access Silicon Nitride Technologies

Rapid Prototyping and Customized Prototyping Services

CENTRO NACIONAL DE MICROELECTRONICA IMB

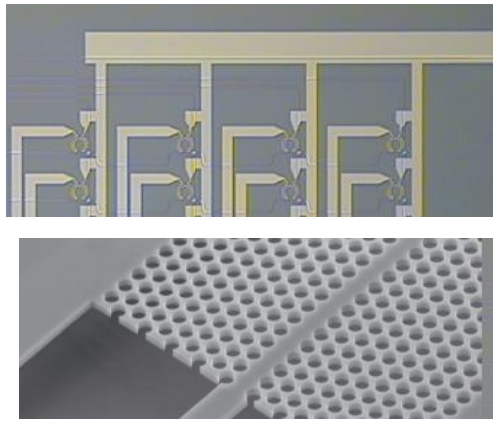


VLC PHOTONICS

300 nm LPCVD SiN

for visible, near and and mid-IR applications

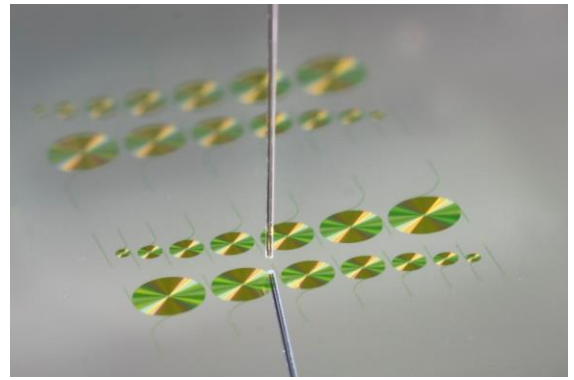
AMO



LPCVD SiN

up to 360 nm layer thickness

CORNERSTONE



UNIVERSITY OF Southampton

LPCVD SiN

300 nm layer thickness

Open source PDK

Prototyping/MPW **Up to 1 K chips or 1 wafer**

LPCVD SiN Platform

High quality LPCVD Si_3N_4

- Design, Process integration, Test
- Stoechiometric SiN
- 200mm wafers with subtractive process
- Cladding opening
- 250nm, 300nm and 800nm thick, other thicknesses on demand with thermal oxide for better thickness control

Record low optical losses

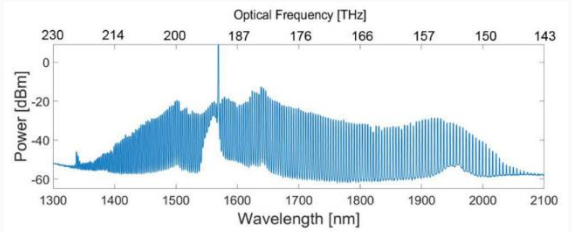
- Ultra-Low loss thanks to smoothing annealing: 0.03dB/cm for tighly confined strip waveguide in S/C/L-bands

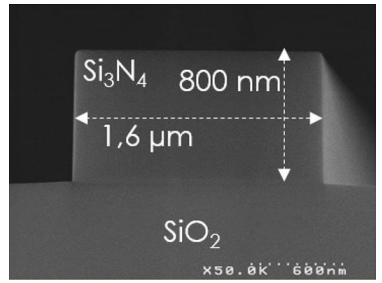
ULLSiN PDK

- 800nm LPCVD SiN PDK including: grating & directional couplers, 1x2 & 2x2 MMI, Y-junction, 10µm bending radius, s-bend, racetrack resonator with Q-factor >5×10^6

APPLICATION from UV to MIR

- Biosensors
- LIDAR
- Quantum photonics
- Non-linear optics, comb generation





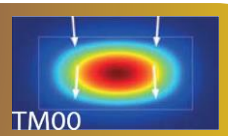
PUBLICATIONS

- S. Boust et al, Microcomb Source Based on InP DFB / Si_3N_4 Microring Butt-Coupling, Journal of Lightwave Technology 2020
- H. El Dirani et al, Ultralow-loss tightly confining Si_3N_4 waveguides and high-Q microresonators, Optics Express 2019

LIGENTEC LPCVD all-nitride core platform

LIGENTEC

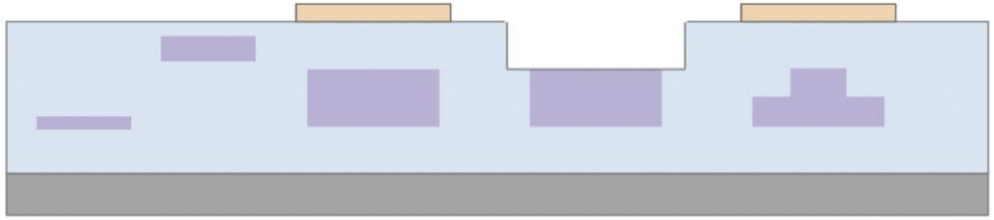
The Basics



- ✓ High Mode Confinement
- ✓ Low Loss (< 0.1dB/cm)
- ✓ Small Footprint (50µm bend)
- ✓ High Power (>10W)

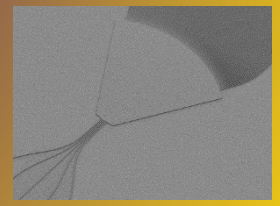
8 MPW/year
Dedicated runs
10 weeks turn around

Flexible R&D line
Volume line



Full Creativity (PDK)

- ✓ Couplers
- ✓ Mux / DeMux
- ✓ MZIs / DLIs
- ✓ Resonators
- ✓ Polarization control

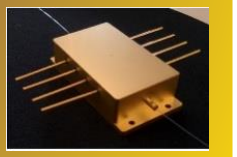


Actives

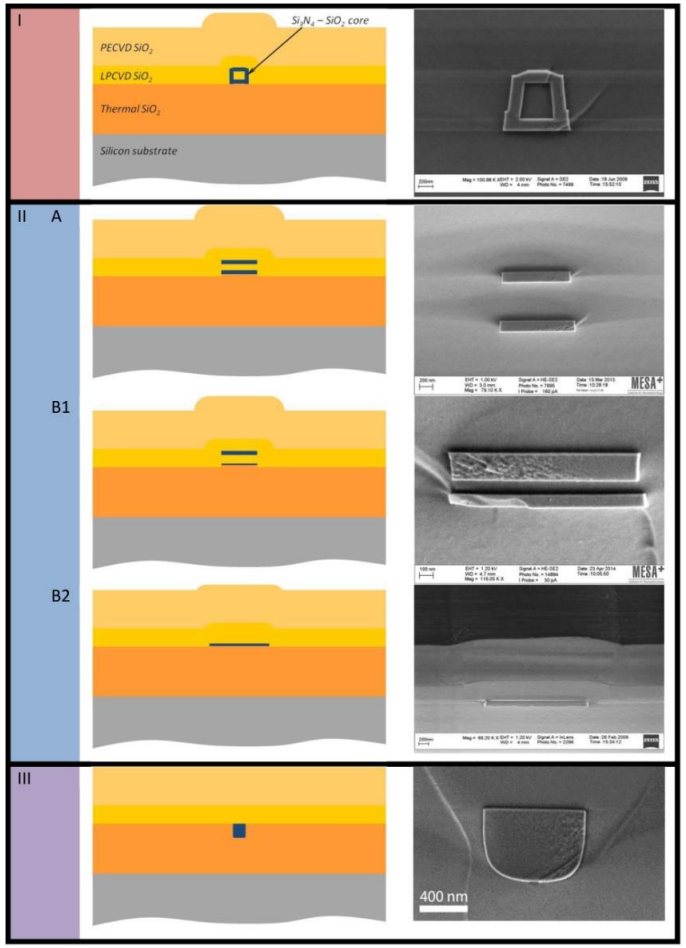
- ✓ Electrical Tuning
- ✓ Modulators (hybrid)
- ✓ Lasers (hybrid)
- ✓ Detectors (hybrid)

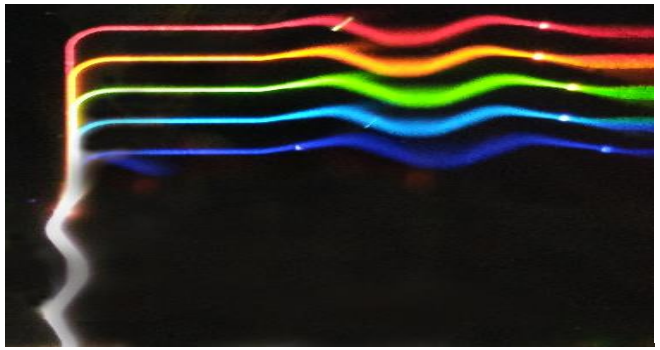
World Connections

- ✓ Edge / Grating Coupler
- ✓ Spot Size Converter
- ✓ Arbitrary Die Shape
- ✓ Bond pads
- ✓ Cladding opening for sensing



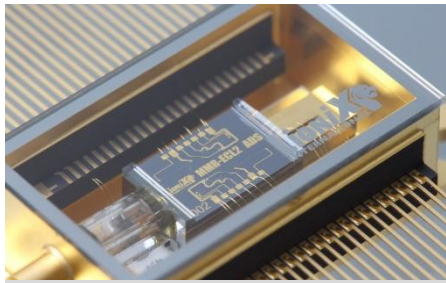
TriPleX™ platform



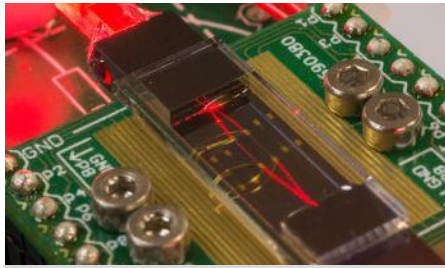


The flexible silicon nitride platform: low loss, wide transparency

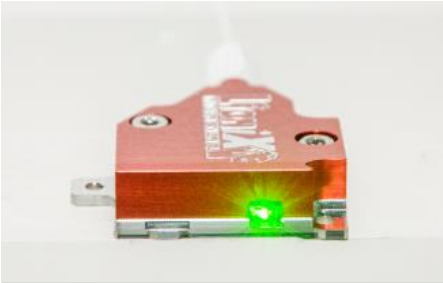
- **Low optical attenuation** from 405-2350 nm
- **Adjustable polarization** properties (sensors, telecom)
- **Small** bend radii (small footprint!)
- **Flexible** properties – geometry by design
- Silicon and glass **compatible**
- Spot size converters for
  - low loss **fiber chip coupling**
  - **hybrid integration**



Telecom/datacom



Life Science



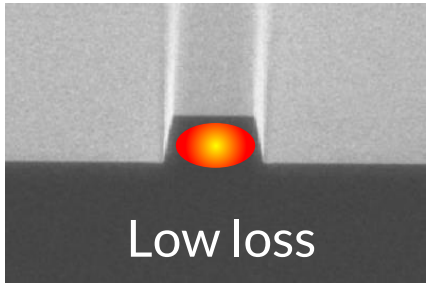
Metrology

TriPleX™: a versatile dielectric photonic platform, Adv. Opt. Techn. 2015; 4(2): 189–207

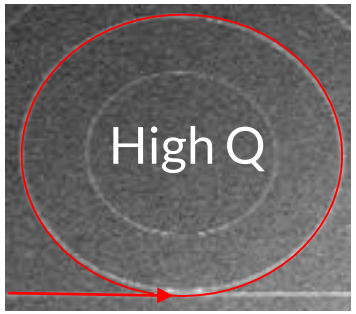
BioPIX PECVD SiN platform

High Performance Passive Devices in SiN Platform

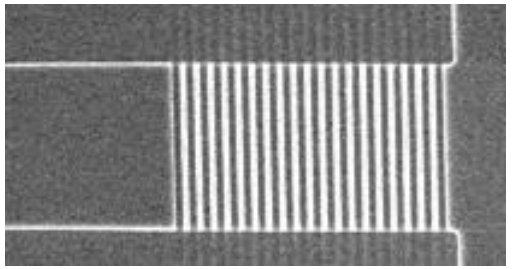
Waveguides



Ring Resonators

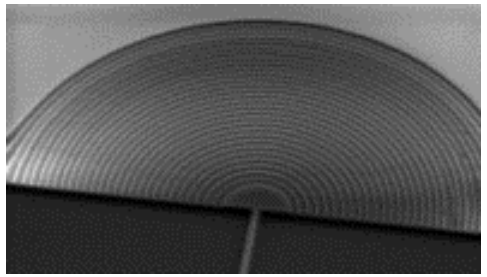


Fiber-WG

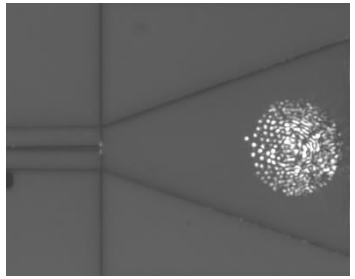


IO-coupler

Focusing

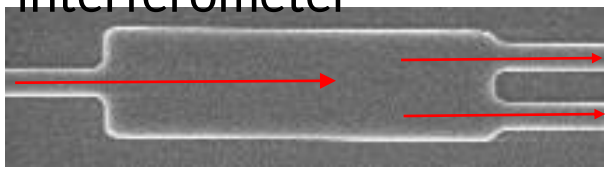


holographic

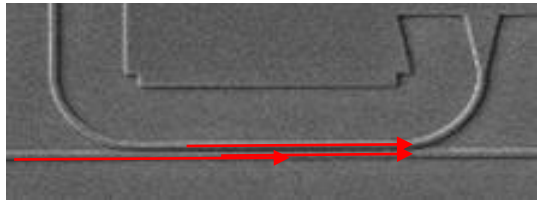


Power splitters

Multi-mode interferometer



Evanescent coupler



CNM SiN photonic platform

The **process technical features**, are:

Wavelength range from Visible to Mid infrared

Three waveguide cross-sections (nitride films 300/340 nm height, shallow 150/300 nm, deep 300 and mini-deep 150 nm)

Thermo-optic tuners (Cr/Au, Poly-Si, Al-5% Cu…High flexibility)

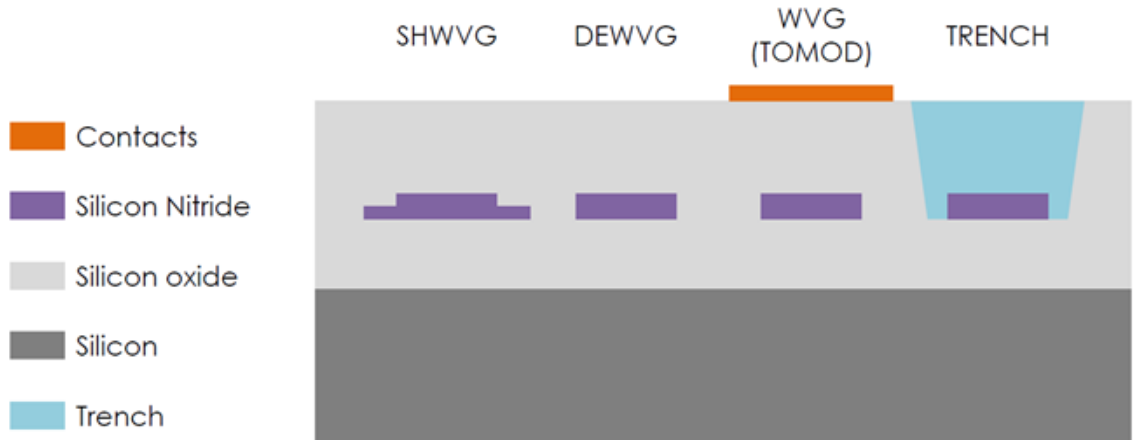
Selective area trenching: integration Biosensors+PICs

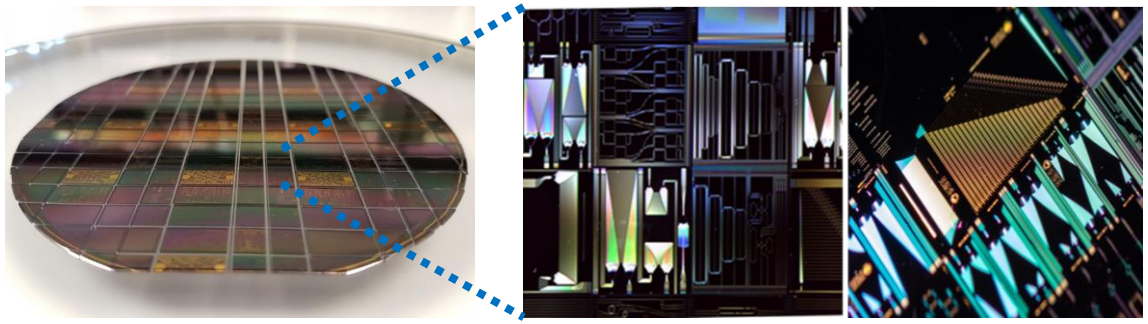
Spot size converters for low loss fiber chip coupling (under development)

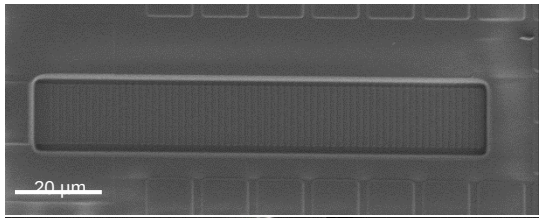
Foundry

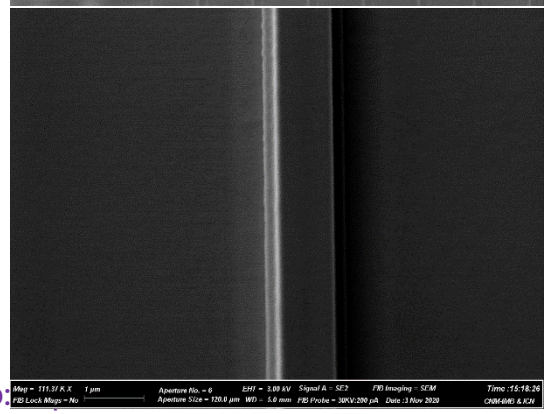
Design
MPW Broker

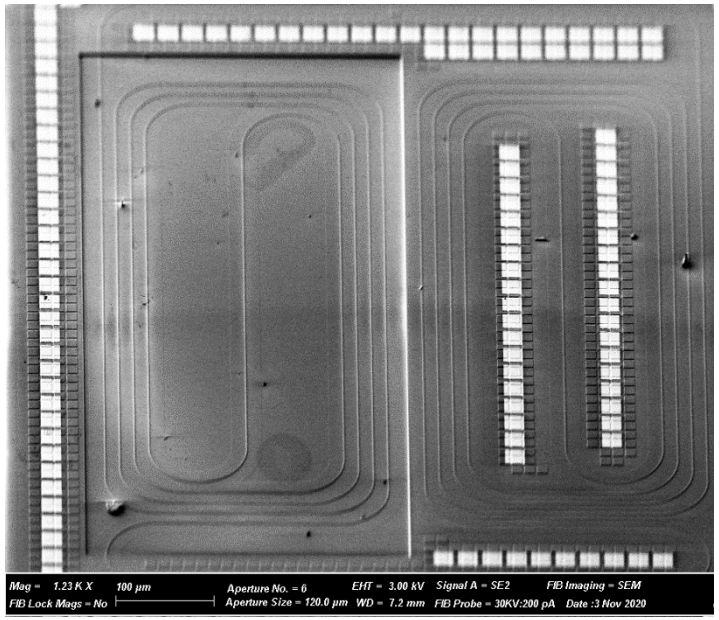
Fabless users



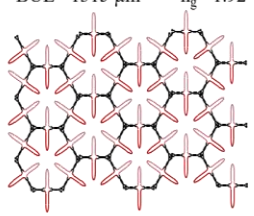


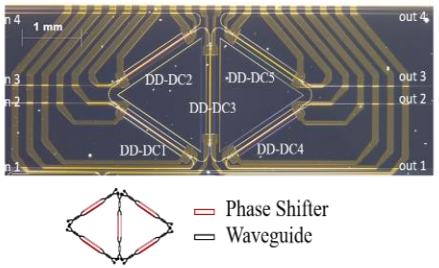






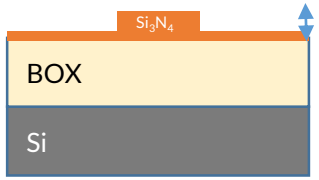
10 Hexagonal Cells size: 5.5 x 11 mm





AMO's LPCVD silicon nitride PICs

LPCVD Si_3N_4 layer thickness: up to 400 nm

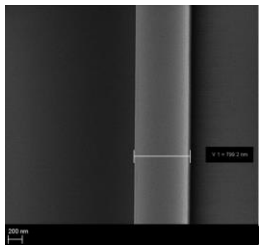


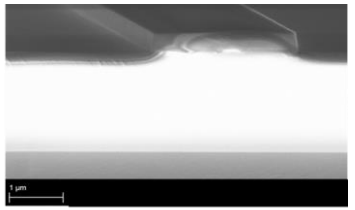
Different BOX-layer thicknesses: i.e. 6 µm, 2.3 µm

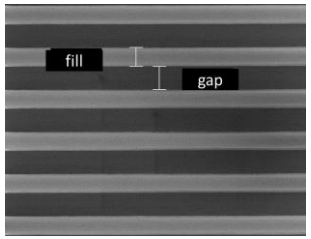
Highly flexible prototyping platform

Wide wavelength range accessible 400 nm-3 µm

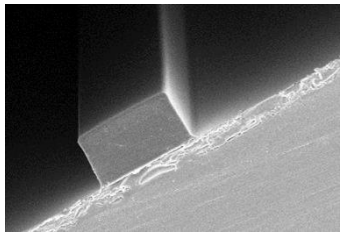
i-line stepper waveguides and grating couplers



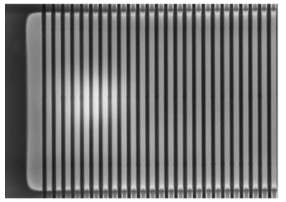




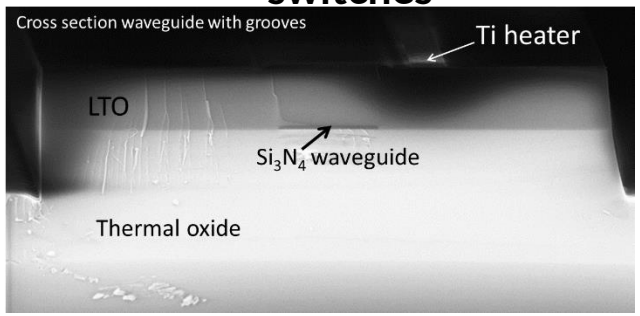
SU8 broad-band spotsize converters

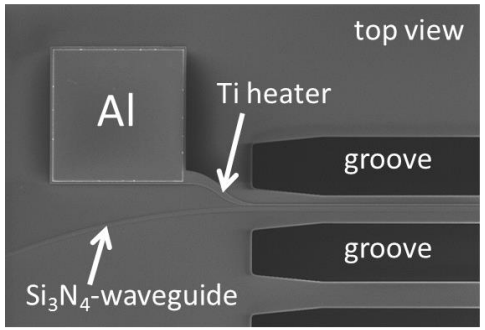


Ebeam grating coupler

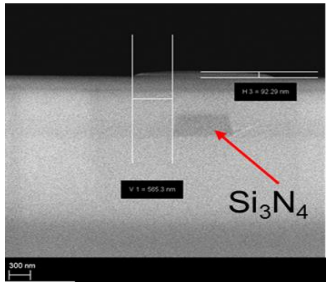


Heaters and thermal optical switches





Cladding planarization



Platform is already in use for:

- **Biosensing**
- **Quantum photonics**
- **Space communication**
- **Integrated lasers**
- **ICT**
- **…**

EUROPRACTICE + CMP : MPW in 6 Silicon Photonics foundries

EUROPRACTICE

- Si-Photonics SiP

- Si-Photonics Si-220
- Si-Photonics Si-310
- SiN-Photonics Si3N4-800

- Si-Photonics 220 nm SOI Passives
- Si-Photonics 220 nm SOI Actives
- Si-Photonics 340 nm SOI Passives
- Si-Photonics 500 nm SOI Passives

- Si-Photonics SG25H5_EPIC

- Si-Photonics iSiPP50G
- Si-Photonics passives+
- SiN-Photonics BioPIX

- SiN-Photonics TriPleX 850
- SiN-Photonics TriPleX 1550
- SiN-Photonics TriPleX VIS

www.europractice-ic.com

Technology Access: IP and licensing

- Most foundries require a license agreement to be signed to access the PDK
- Typical IP assignment:
  - Foundry owns manufacturing IP and know-how
  - Foundry may own IP protected black-box components/designs
  - Designer may own new device design IP
    - IP is maintained by ensuring that other users on an MPW run do not see your designs
    - An NDA is often signed with all parties
- Foundries often have a model in place for IP licensing
- Technology transfer between foundries (i.e. for ramp-up in volume) can be challenging

Current status of open-access foundry services

Attribute	Status
Application spectrum of silicon photonics PIC platforms	Visible to mid-IR, myriad applications
Maturity of Silicon Photonics Platforms	High
MPW turnaround time	3 to 6 months
Prospects for scaling up volumes by European fabs	Low to medium volume manufacturing possible
Prospects for high-volume manufacturing in Europe	Currently only in partnership with non-EU fabs
Brokerage services for Silicon Photonics MPW	Possible
Design support	Possible
Training, education and skill development	Possible

You need more than just a fab

- Design and simulation tools: the market is evolving

- Packaging: strong progress is past several years

GET IN TOUCH

Abdul Rahim, Ph.D
Coordinator

Prof. Roel Baets
Chairperson

William Chen, Ph.D
China Liaison Officer

http://epixfab.eu info@ePIXfab.eu +32 9 331 4843 /groups/4888115