Evolutions in Silicon Photonics
Technology platforms, Services and Tools

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Lars Zimmermann (IHP)
Maryse Fournier (Leti)
Peter O'Brien (Tyndall)
Timo Aalto (VTT)
Iñigo Artundo (VLC Photonics)
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Outline

- Recent developments by silicon photonics design tool developers
  - Luceda IPKISS
  - PhoeniX
- Updates from the technology providers
  - imec
  - IHP
  - LETI
  - VTT
- Packaging service at Tyndall and design service by VLC Photonics

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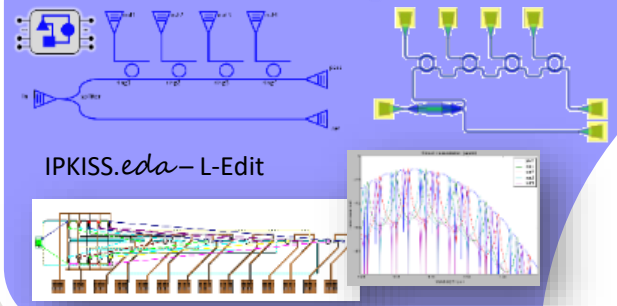
LUCEDA: Design flow integration and scalability

Circuit drives layout – drives simulation



IPKISS.*eda* – L-Edit

PDKs and Libraries

imec

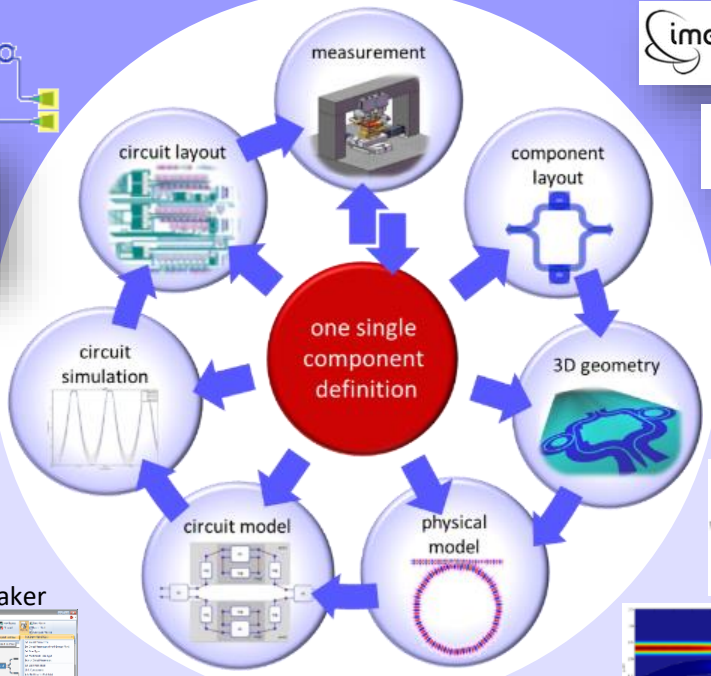
IME A*STAR

ihp

VTT

Tyndall National Institute

PICAZZO

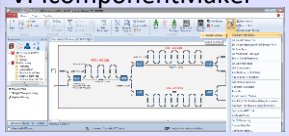


System Simulation

IPKISS-CAPHE

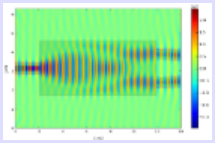
```
links = {# input coupler to splitter
         ("gc_in:port_1",     "splitter:port_1"),

         # splitter to reference
         ("splitter:port_2", "gc_ref:port_1"),

         # connecting the rings together
         ("splitter:port_3", "ring1:in1"),
         ("ring1:out1",      "ring2:in1"),
         ("ring2:out1",      "ring3:in1"),
         ("ring3:out1",      "ring4:in1"),
         ("ring4:out1",      "gc_pass:port_1"),
```

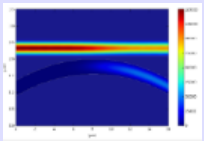
VPIcomponentMaker



Physical Simulation

3D modal solver

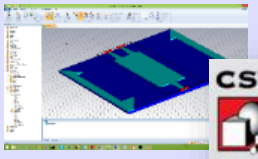




RMIT UNIVERSITY

IPKISS CAMFR

CST Studio Suite

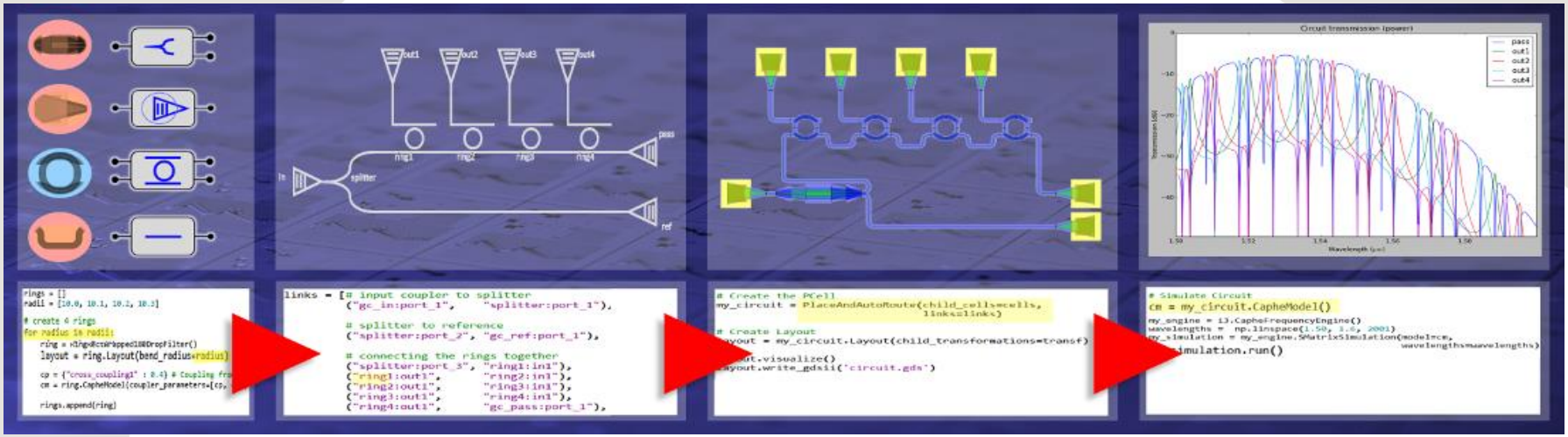


CST

LUCEDA

IPKISS.*flow* 3.1 Raises the integrity of your design flow

Component libraries | Circuit | Circuit driven layout | Layout driven simulation



- ✓ fully parametric powerful Python scripting
- ✓ from netlist to layout in the same component
- ✓ circuit simulation & validation by measurement
- ✓ customizable to internal design methodology

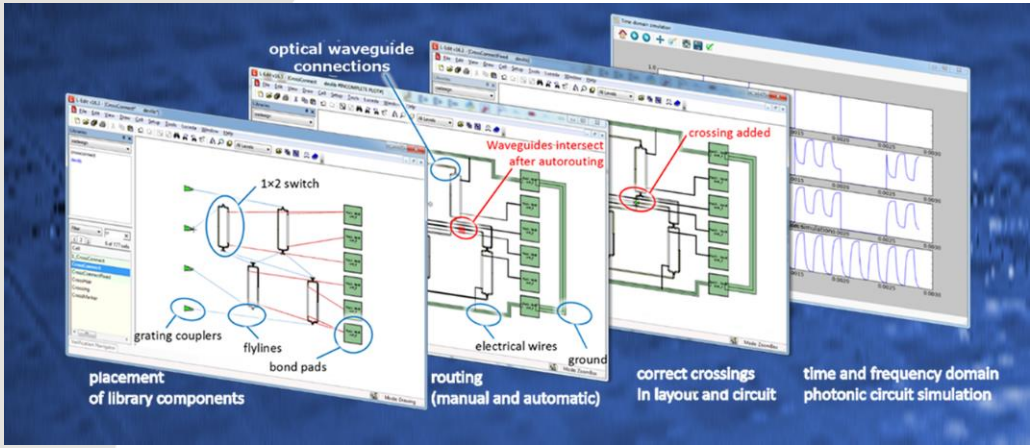
- ✓ **Reduces design errors:**
  fully coupled layout & circuit simulations.
- ✓ **Integrates your flow:**
  Interfaces with system & physical simulation
- ✓ **Saves time:**
  the Picazzo library with layout & circuit models

LUCEDA

IPKISS.eda 3.1: Full control over your PIC design embedded in Tanner L-Edit

IPKISS.eda for Tanner L-Edit by Mentor Graphics

Mentor Graphics



- IPKISS.flow + L-Edit
- intuitive, visual, easy, fast
- photonic & electric drag-drop & route

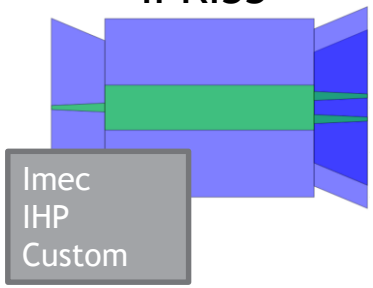
- ✓ Quickly prototype my circuit
- ✓ Make my design as compact as possible
- ✓ Do electrical routing
- ✓ Detect layout effects - include them in calculations
- ✓ Build complex devices
- ✓ Make my designs DRC free

LUCEDA

IPKISS-CST link for Integrated Photonics

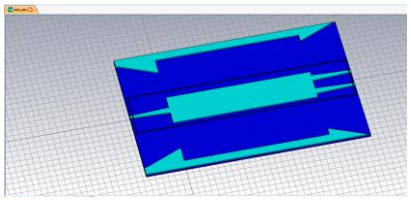
IPKISS

IPKISS

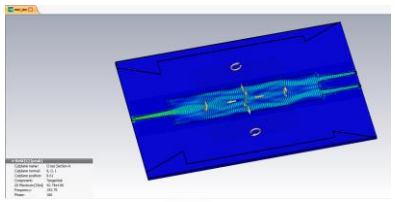


CST STUDIO SUITE

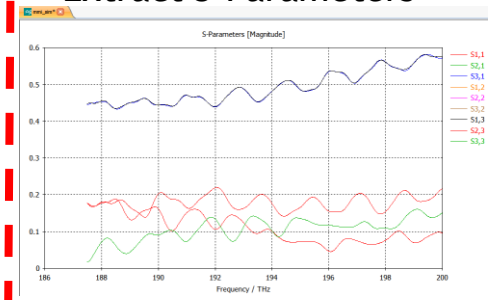
CST Model



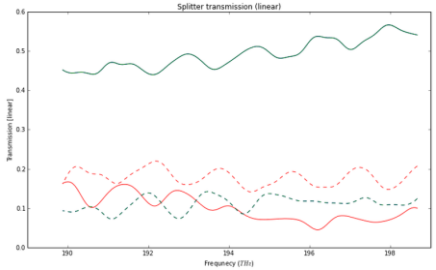
CST Simulation



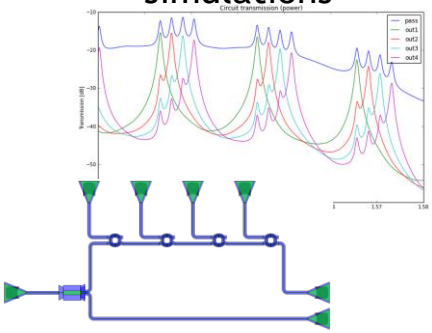
Extract S-Parameters



Import model in IPKISS

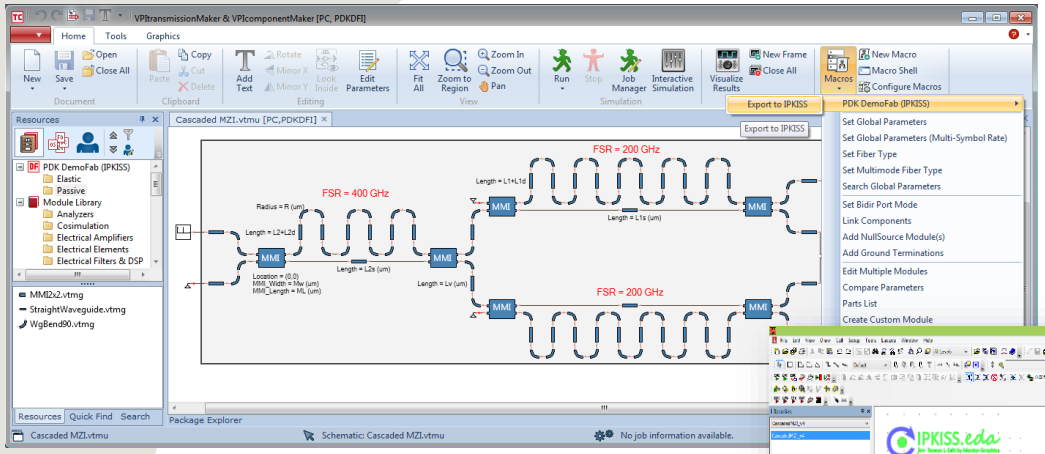


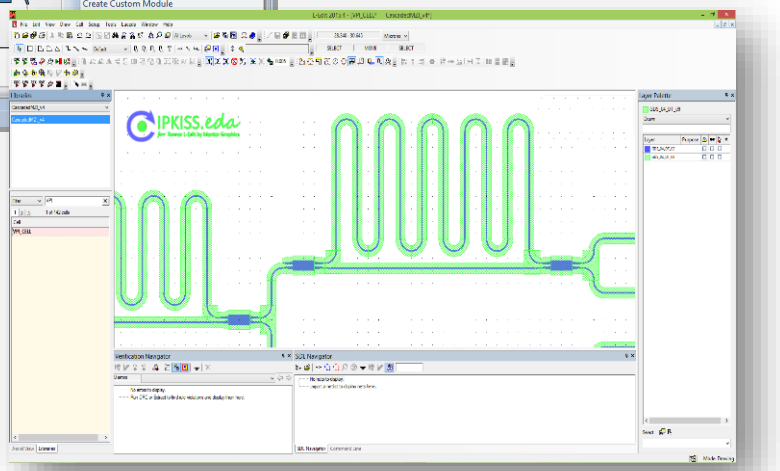
Use model circuit simulations



CST: FIT/FDTD, FEM, Thermal, …) in a single GUI

VPIcomponentMaker Photonic Circuits Cross-Connect IPKISS.eda





- ✓ High flexibility
- ✓ Easy customization

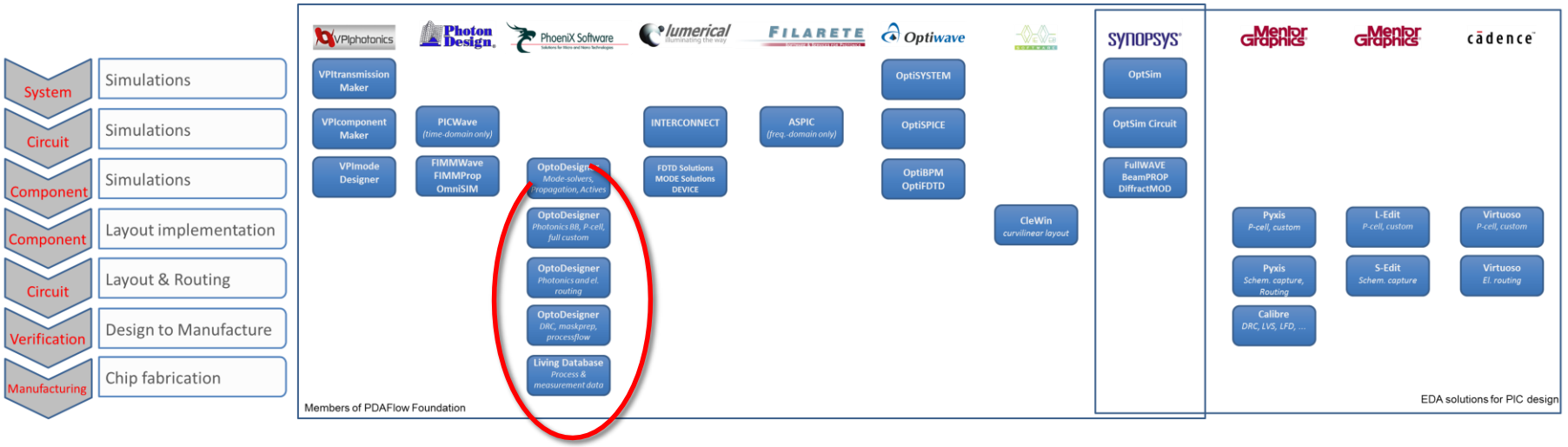
Fast implementation of fab-specific IPKISS-based photonic Process Design Kits on circuit and layout design levels.

VPIphotonics DESIGN AUTOMATION

LUCEDA

PhoeniX Software

creating integrated photonic IC design flows



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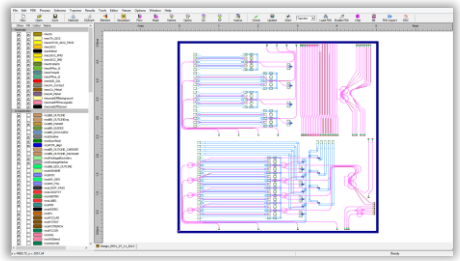
OptoDesigner 5, photonic IC design suite

Chip and mask layout



- Native curvilinear and all angle design
- Complete parametrized library for photonic elements, components and devices
- Photonic Synthesis based on technology parameters and design intent
- Verification, DRC and Routing (electrical, optical, constraint based, …)

Photonic simulations

- Circuit simulations (by ASPIC or internal), Mode-solvers and Propagation simulations (BPM, EME, FDTD)

Flexible Import and Export capabilities

- Interfaces with circuit tools from Filarete, Lumerical, VPIphotonics and Photon Design
- Integration with CleWin and EDA tools from Mentor Graphics and Cadence
- Raith e-beam writer export (FBMS)

Easy to use GUI including powerful domain specific scripting

- Efficient, fast and mature

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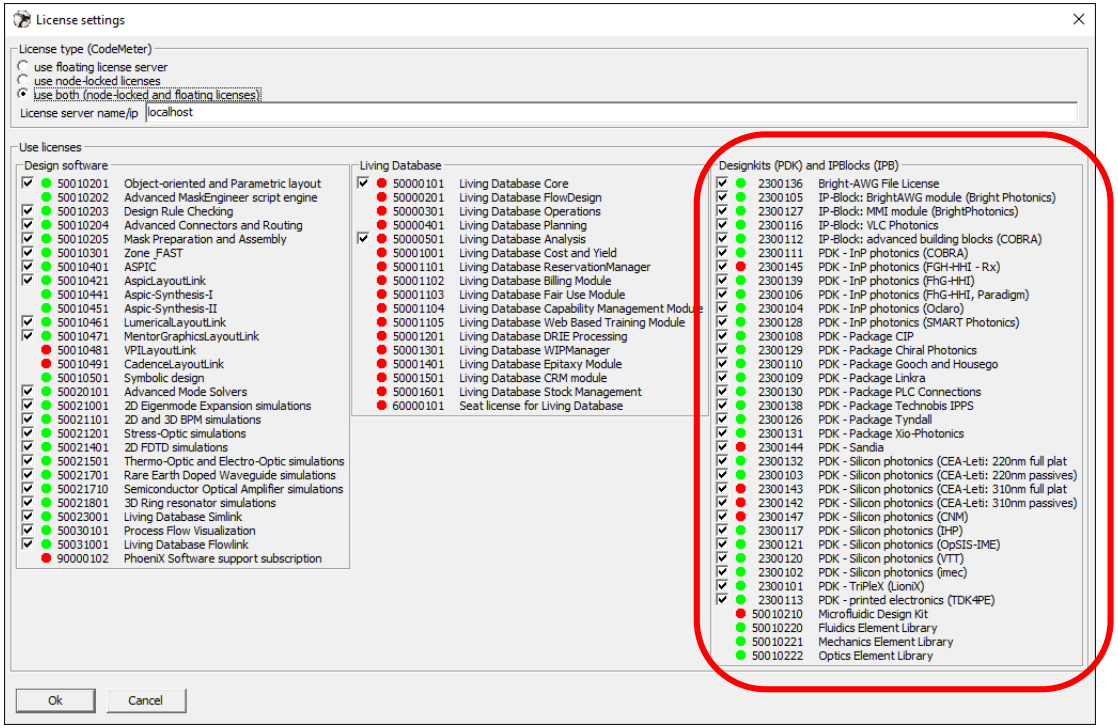
OptoDesigner supports any photonic platform

Compatible with Process Design Kits (PDKs)

- 10 photonics foundries offering MPW services are available, also packaging templates



Adding a new PDK in OptoDesigner takes hours or days, not weeks. Training every February in PhoeniX HQ.

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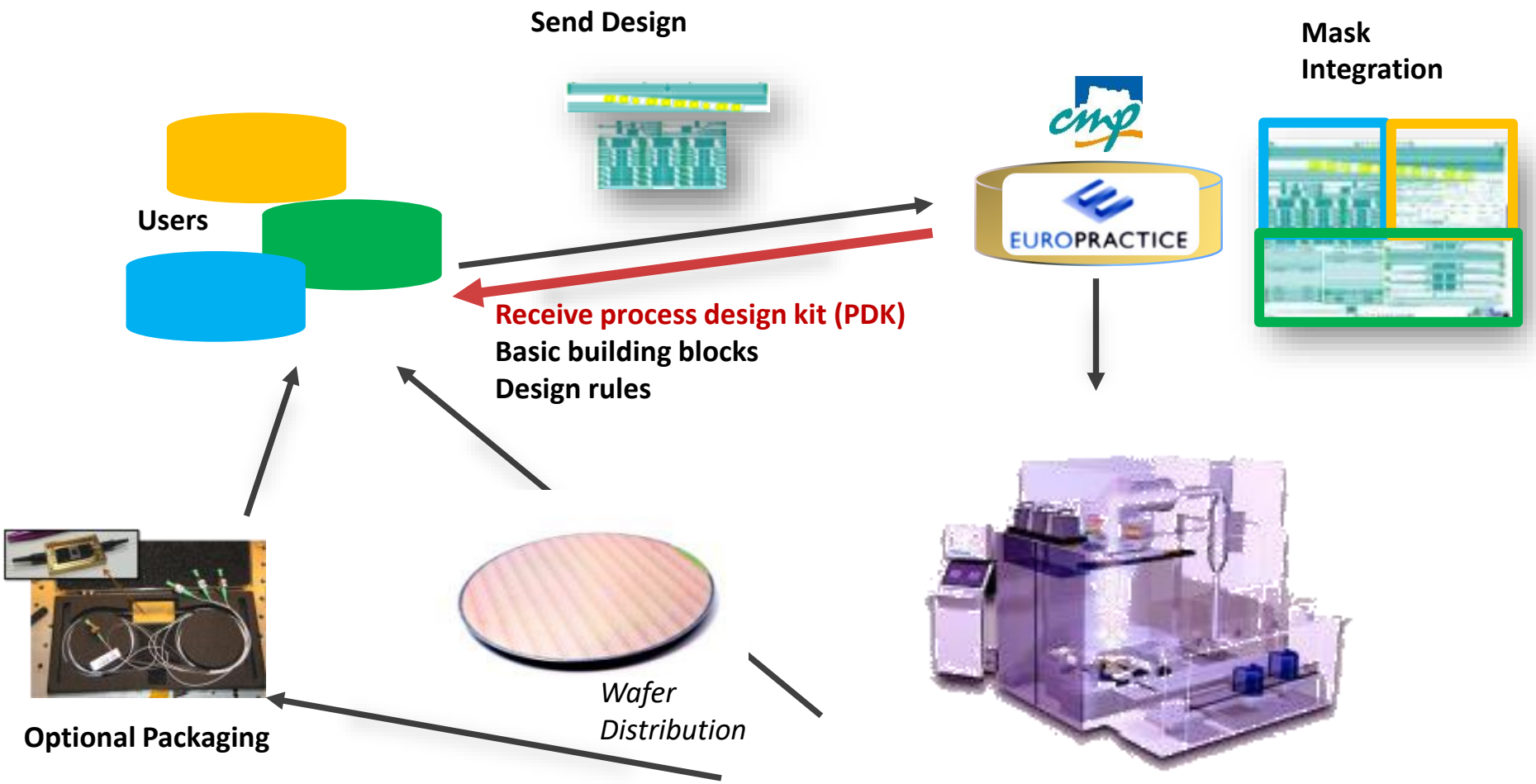
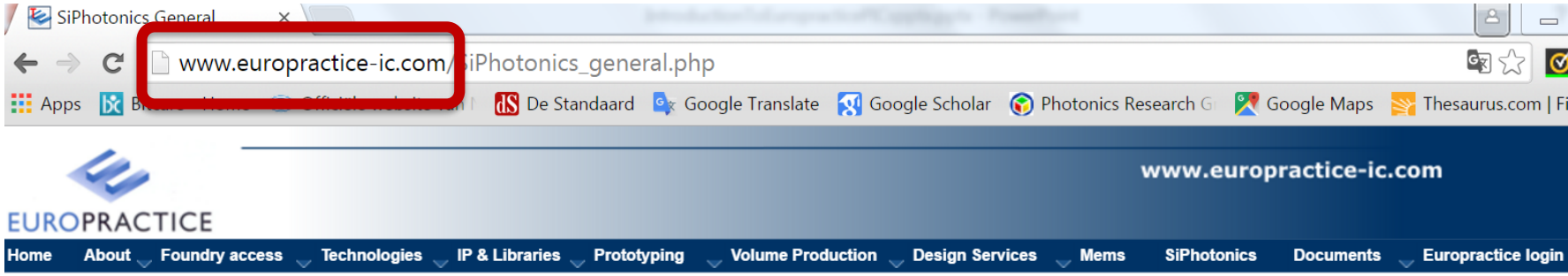
Cost-sharing of multi-project wafer runs




SiPhotonics General
www.europractice-ic.com/SiPhotonics_general.php
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General
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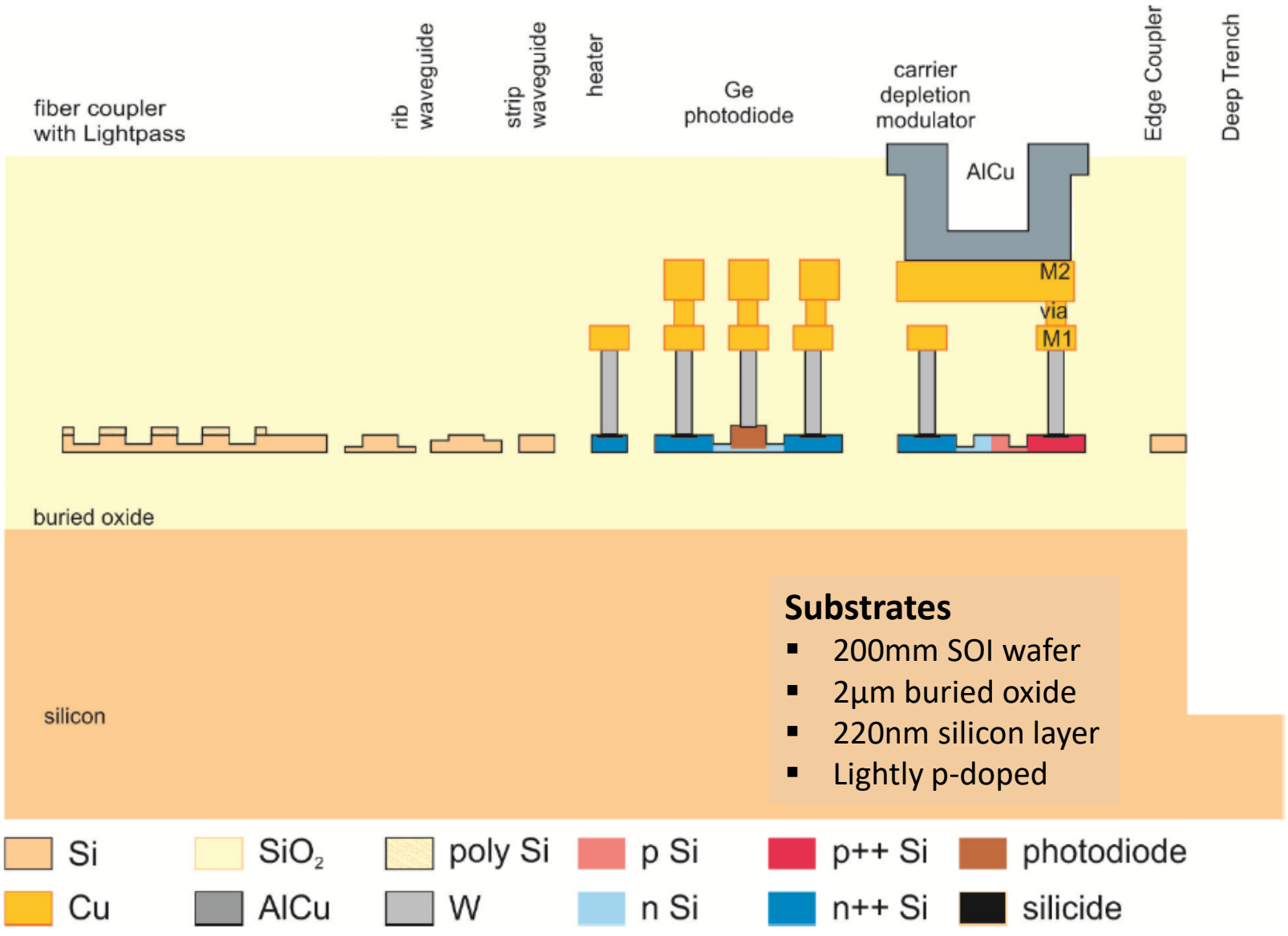
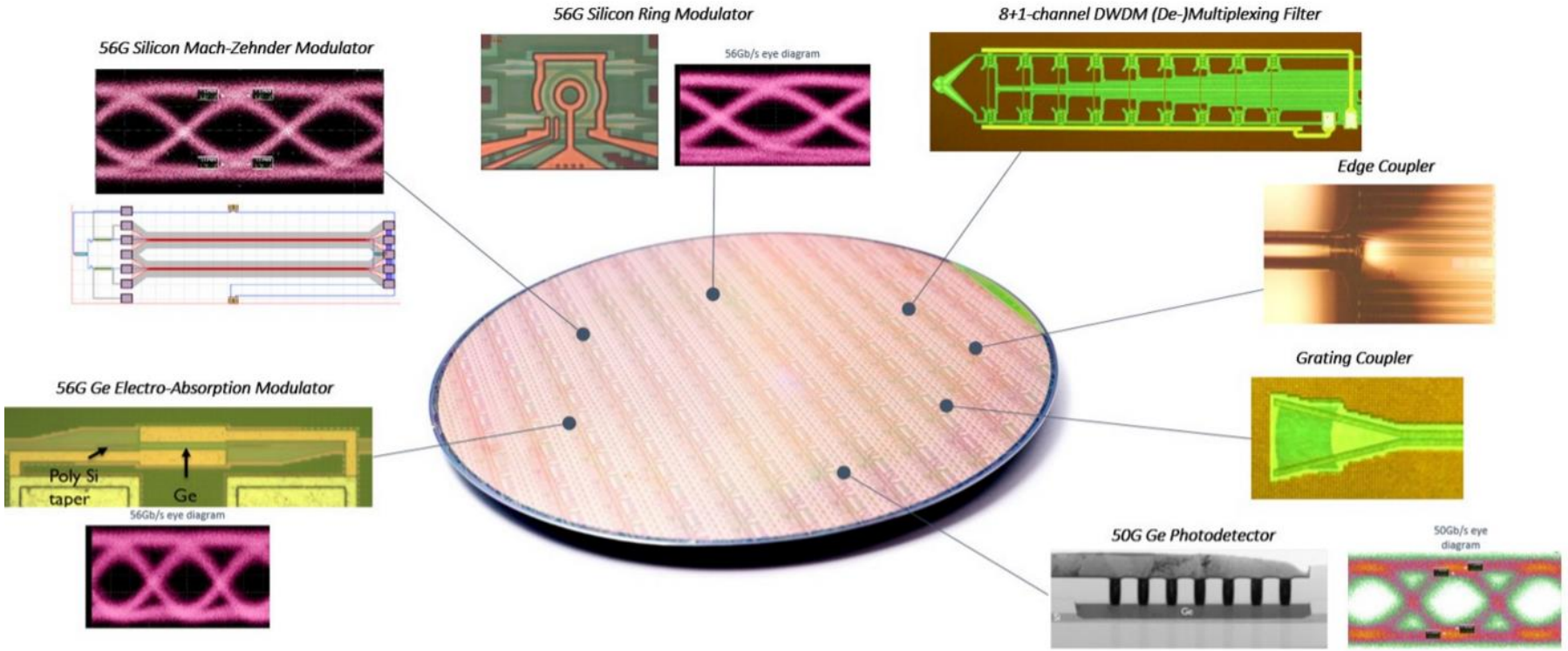
Technology
imec - Passives
imec - ISIPP25G+
LETI-Passives with Heaters
IHP-Passives Ge photodiode
Runschedule & Pricing
Runschedule
Pricing
NDA-DKLA
Info
Design info
Practical info
NDA-DKLA
Photonics Packaging
Technology description
Packaging Prices
Europractice Silicon Photonics MPW offer
Technologies
For Silicon Photonic IC prototyping, EUROPRACTICE currently offers the following technologies through MPW service:
imec-ePIXfab SiPhotonics: passives
imec-ePIXfab SiPhotonics: ISIPP25G
LETI-ePIXfab SiPhotonics: passives with heater
IHP SG25 PIC SiPhotonics: passives Ge photodiode
EUROPRACTICE offers access to MPW services for non-commercial use by universities and research centers. For commercial use, EUROPRACTICE will bring you in direct contact with the foundry.
Support
EUROPRACTICE offers support by way of :
Technology information, design rules, design templates, ...
Design kit for SiPhotonics CAD software (layer file, DRC, basic libary, etc.)
Access to low cost CAD tools for Photonics design through Europractice software.
Special discounted prototype fabrication prices
ePIXfab is the European silicon photonics R&D foundry initiative. Europractice works closely with ePIXfab to implement the SiPhotonics MPWs.
ePIXfab also offers additional support:
Training and tutorials
Packaging service

ISIPP25/50G platform of imec



Mid Nov. a new PDK with 50 Gb/s components will be released



Imec's active iSiPP50G run is now open for registration (deadline Oct. 31st 2016)

LUCEDA PHOTONICS

http://www.lucedaphotonics.com/

PhoeniX Software
Solutions for Micro and Nano Technologies

http://www.phoenixbv.com/

ISIPP25/50G modules

MPW Access:
Amit Khanna: epsiphot@imec.be
T +32 468 33 29 05
www.europractice-ic.com

Modules	Description	Enabled devices
3 silicon patterning steps	3 etch depths in 220nm Si: 70nm, 160n; 220nm (193 nm litho)	Strip/rib waveguides, various passive optical devices, silicon taper
Gate oxide and Poly-Silicon layer	1 etch depth: full poly etch (160nm) (193nm litho)	Advanced grating couplers, poly-Si wave-guide
Ion implantation in Si	6 implants levels: 3x n-type and 3x p-type	Si carrier depletion, injection and ac-cumulatin devices, Ge Photodectors, doped Si resistors, ...
Ge module	100% Ge(Si) RPCVD se-lective epitaxial growth & 2x implants levels	Ge Photodectors Ge(Si) EA modulator
Silicide tungsten contact module	Ohmic contacts to doped silicon	Standard CMOS con-tacts plugs, Tungsten heater
Two-level metal inter-connect	Cu-based two-level metallization	Standard CMOS interconnects
Aluminum passivation	Aluminium finish metallization	Standard CMOS interconnects
Deep trench	Deep trench to expose edge coupler facets	Edge couplers

Typical performance level: passives

PASSIVES (typical performance values)

Single Mode Waveguides		Typ.Value	Unit	Comments
Strip Waveguide C-band		<2.0	dB/cm	450nm wide
Strip Waveguide O-band		<3.0	dB/cm	380nm wide
Rib Waveguide C-band		<1.0	dB/cm	650nm wide
Rib Waveguide O-band		<1.5	dB/cm	580nm wide
Thickness Control	3σ	<4.5	nm	
Fiber Grating Couplers		**Type.Value**	**Unit**	**Comments**
Insertion Loss		2.5	dB	C-band*, TE, SMF
I dB Bandwidth		29	nm	C-band*, TE
Peak-λ within-wafer control	1σ	<4	nm	
Fiber Edge Couplers		**Typ.Value**	**Unit**	**Comments**
Insertion Loss		<2	dB	C-band*, Lensed Fiber
I dB Bandwidth		>100	nm	C-band*
Polarization dependent loss		<0.5	dB	C-band*

* O-band versions available in PDK

Typical performance level: actives

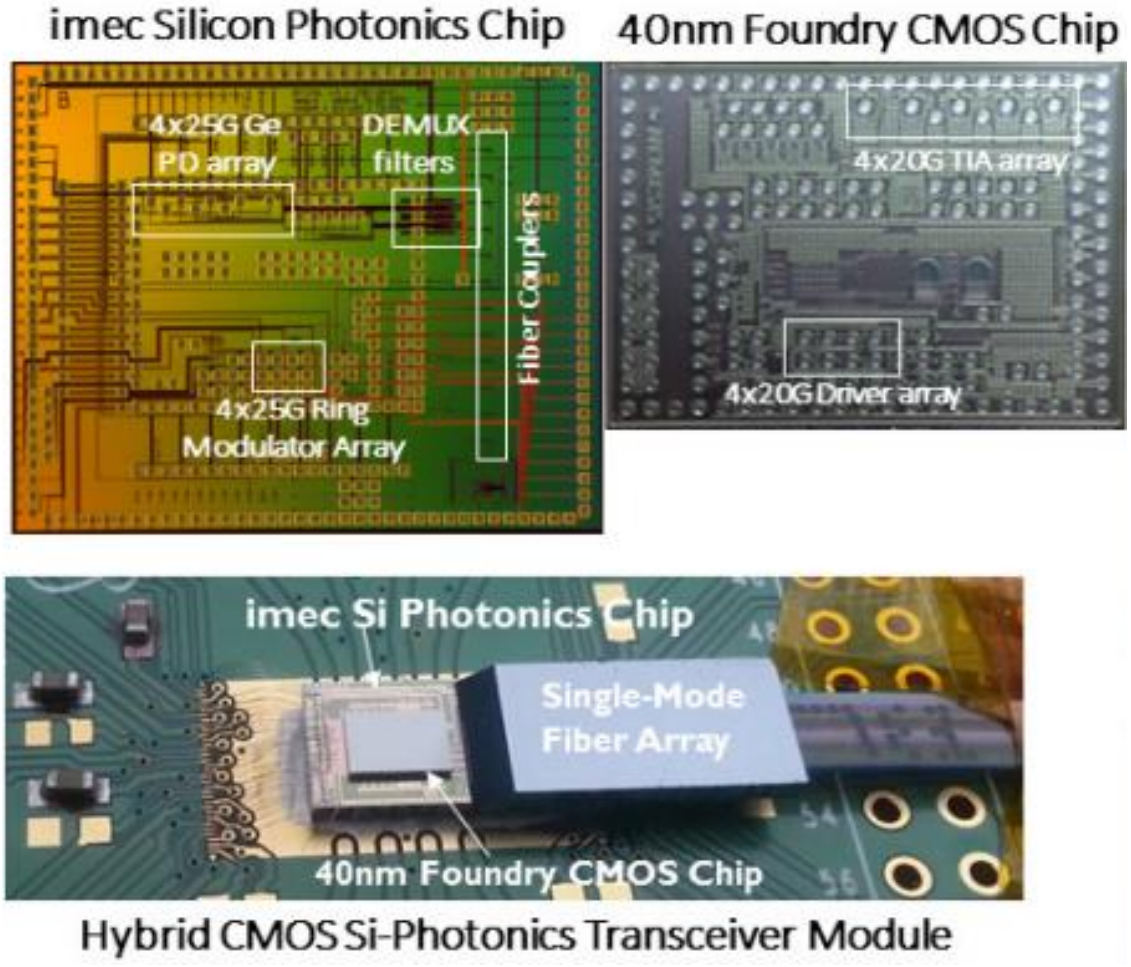
50G SI RING MODULATOR (typical performance values)

Parameter		Typ.Value	Unit	Comments
Operation Wavelegnth		~1550	nm	O-band version also available (40Gb/s)
Quality Factor	Q	2000-3500		Low Q - Medium Q
Electro-Optic Bandwidth (S21)	f3dB	~35	GHz	Medium Q (0V bias)
		~47	GHz	Low Q (0V bias)
Static Transmitter Penalty	TP	10-11	dB	Medium Q - Low Q (1.5Vpp drive swing)
Diode Capacitance	Cj	20-30	fF	
Diode Series Resistance	Rs	~70	Ohm	
Ring Radius	R	5	um	

50G GE PHOTODETECTOR (typical performance values)

Parameter (type 1)		Typ.Value	Unit	Comments
Opto-Electrical Bandwidth	f3dB	>50GHz	GHz	C-band
C-band Responsivity		~0.88	A/W	
O-band Responsivity		~0.85	A/W	
Dark Current	Id	<50	nA	
Parameter (type 2)		**Type.Value**	**Unit**	**Comments**
Opto-Electrical Bandwidth	f3dB	>25GHz	GHz	C-band
C-band Responsivity		~1.0	A/W	
O-band Responsivity		~0.94	A/W	
Dark Current	Id	<50	nA	

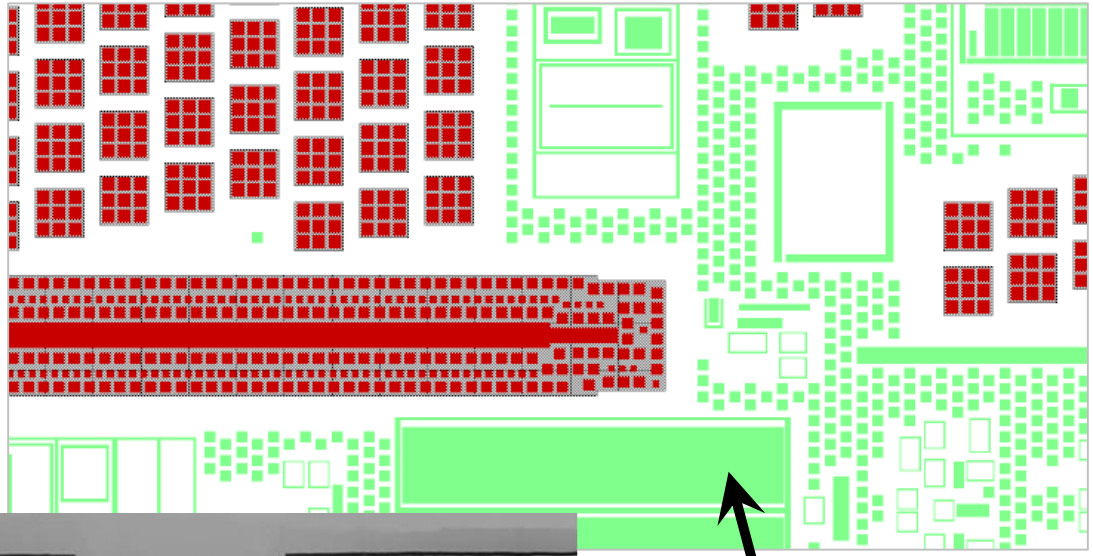
Technology demonstrator: 4x20 Gb/s DWDM



M. Pantouvaki et al, 50 Gb/s Silicon Photonics Platform for Short-Reach Optical Interconnects, Optical Fiber Communication Conference 2016 (**invited**), United States, p.Th4H.4 (2016)

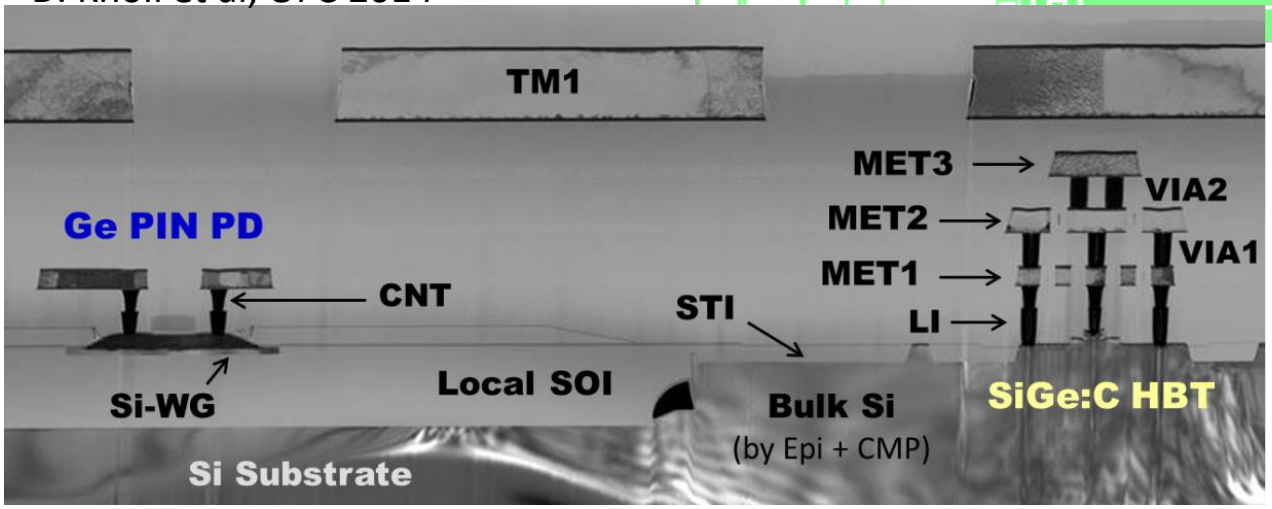
German ePIC technology – photonic BiCMOS (@IHP)

- Monolithic approach
- Mixed Substrate:
  - Localized SOI areas for optical structure
  - Bulk like substrate for BiCMOS structures
- Common backend



Green: Active
Red: Waveguide
White: STI
Grey: local SOI

D. Knoll et al, OFC 2014



L. Zimmermann, *Monolithic Electronic-Photonic Co-Integration in Photonic BiCMOS*, W3F5, ECOC, 2016

Booth # 350 @ ECOC

Technology summary

Photonic features

- 3 etch levels (220nm, 70nm, 120nm)
- 4 dopings (p+, n+, p, n)
- Germanium photodiode (fixed building block)
  - f_{3dB}>65GHz@-2V
  - R>0.9A/W
  - I_{dark}<100nA@-1V
- Phase Shifter (cross section)
- Grating Coupler (4dB@1.55µm)
- Waveguides
  - Loss<2.4dB/cm (220nm etch, λ=1.55µm)
  - Loss<0.7dB/cm (70nm etch, λ= 1.55µm)

Substrates

- 200mm SOI wafer
- 2µm buried oxide
- 220nm silicon layer
- Lightly p-doped
- Resistivity 10Ωcm

SiGe HBT from SG25H4		
f_{max} (GHz)	f_T (GHz)	BV_{CE0} (V)
220	180	1.9
190	190	2.2

Common features

- Backend metal (AlCu, 5 layers)
- Localized backside etching (optional)

Booth # 350 @ ECOC

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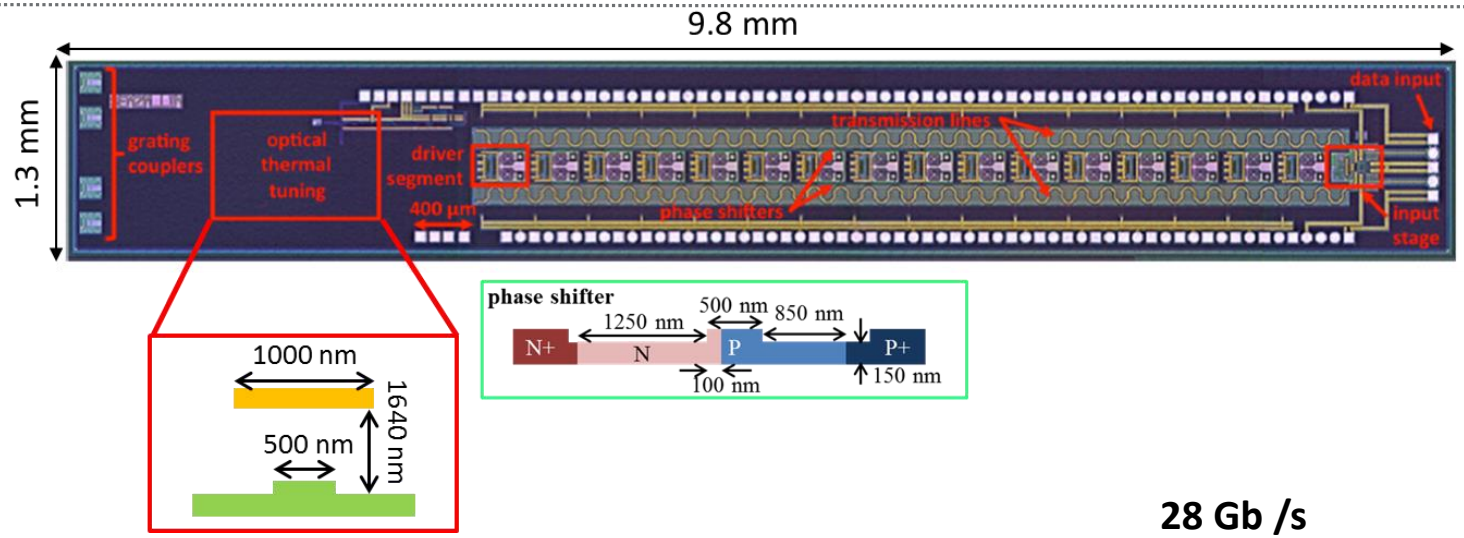
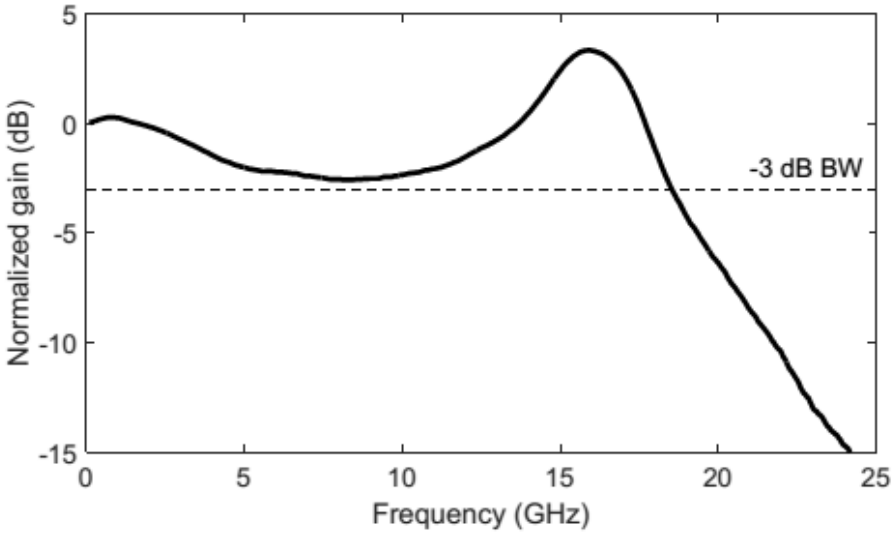
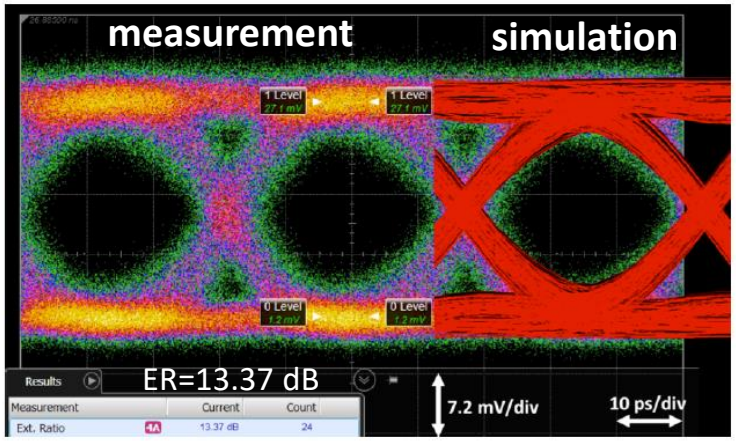
Segmented modulator





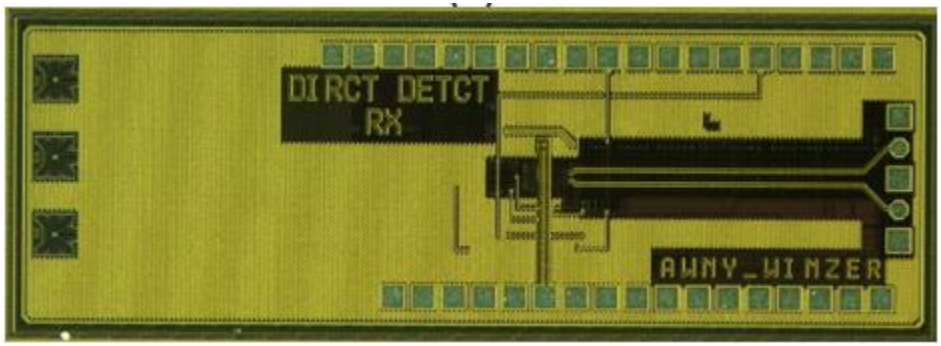
28 Gb /s

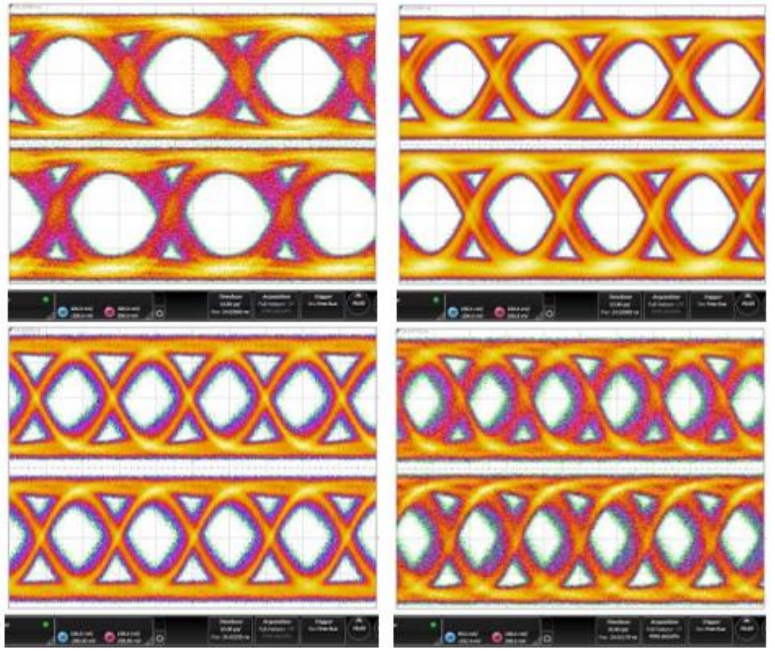


D. Petousi et al, *Monolithic Photonic BiCMOS Sub-System Comprising Broadband Linear Driver and Modulator Showing 13 dB ER at 28 Gb/s*, **CLEO, 2016**

Booth # 350 @ ECOC

Preliminary results – linear SP receiver





- Receiver up to 56Gbps
- Extended BW

M. Kroh et al, *Monolithic Photonic-Electronic Linear Direct Detection Receiver for 56Gbps OOK*, **ECOC 2016**

Booth # 350 @ ECOC

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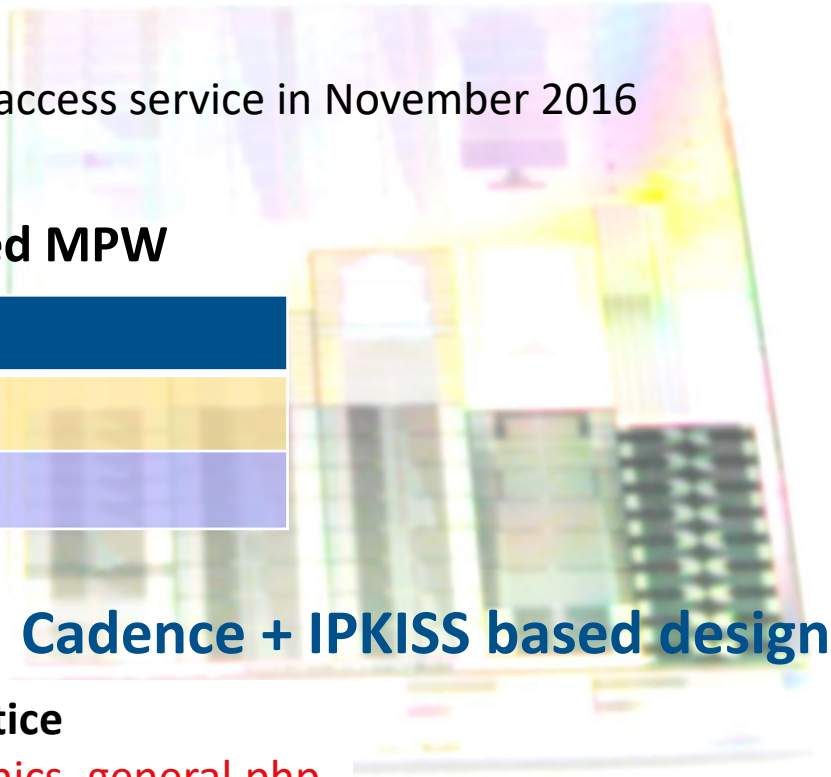
IHP MPW service

Photonic BiCMOS joins the IHP MPW portfolio

- More than 10years of MPW support
- First public photonic-electronic early access service in November 2016



Current IHP photonic BiCMOS related MPW

Technology	Tape-In Deadline
SG25H_EPIC	November 07, 2016
SG25H4	August 08, 2016

Note:
(1)You need to sign an NDA with us.
(2) Register designs well in advance.

Cadence + IPKISS based design-kit

Technology is also available via Europractice
http://www.europractice-ic.com/SiPhotonics_general.php

Additional Information + Terms & Conditions
http://www.ihp-microelectronics.com → Services → MPW & Prototyping

Booth # 350 @ ECOC

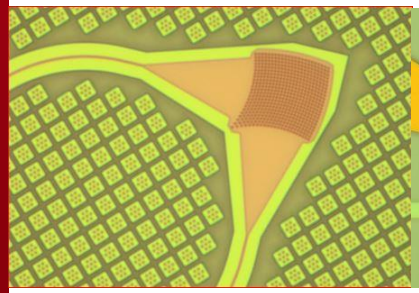
DE LA RECHERCHE À L'INDUSTRIE

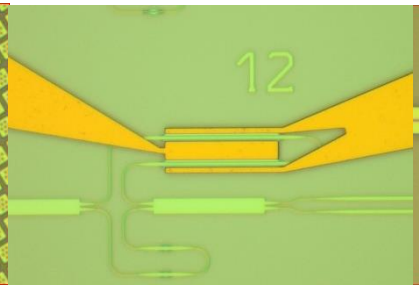
www.cea.fr

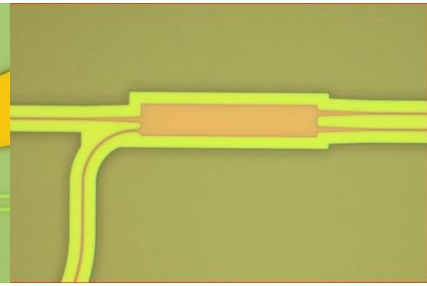
CEA LETI' MPW ACTIVITY

SOI310-PHMP2M FOR PHOTONIC INTEGRATED CIRCUIT

LETI CONFIDENTIAL | **Fournier Maryse**







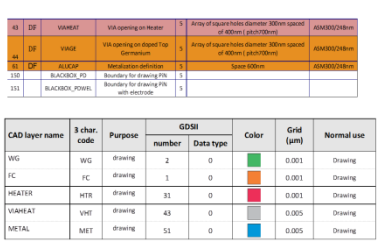
NANOELEC

September 18th, 2016

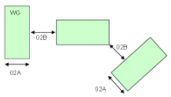
Our Design tool environment & Circuit development

DRM including packaging rules, library and photonic design Kit

- Development of a reference PDK containing all layout information

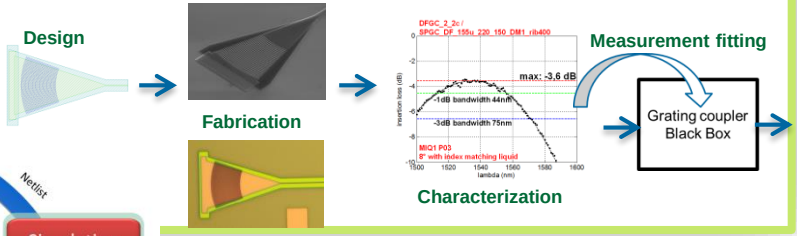


Process Design Kit context (DRM):
Choose rules in the global offer (Léti DRM).
Define the minimum or unique value for each design rule



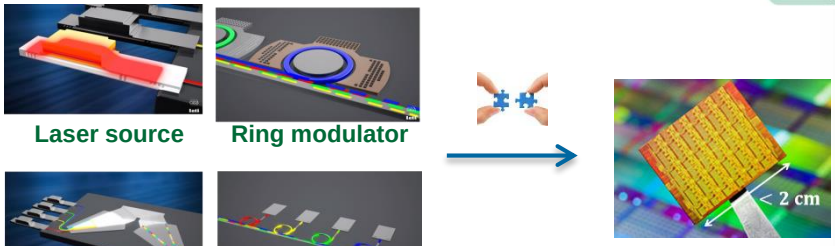
Building the library : component modeling

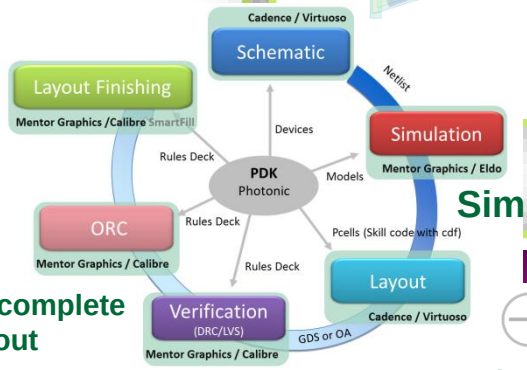
- Creation of component analytical models based on measured behavior
- Parameterization of these models by final user to fit with design constraints



From simple components… to complete integrated systems

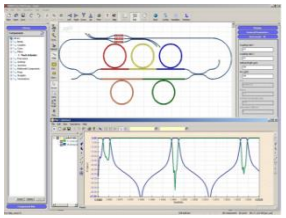
- Putting things together : simulation of complete circuit, design rule checking and tape-out





Simulation with user-friendly interfaces

- Our libraries are compatible with CADENCE IDE using the Eldo simulator and with ASPIC from the Phoenix software suite



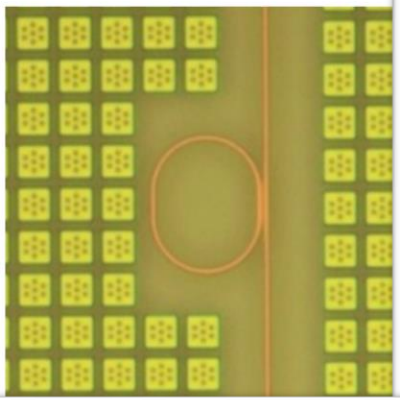
cadence® Mentor Graphics

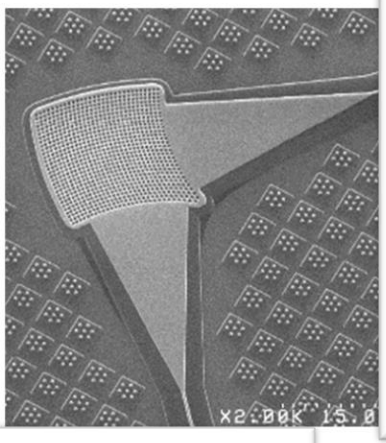
PhoeniX Software
Solutions for Micro and Nano Technologies

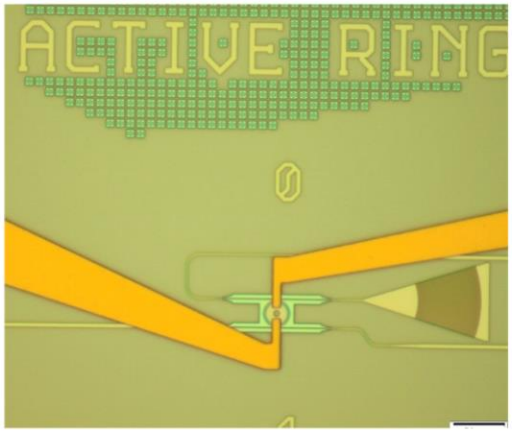
Booth # 397 @ ECOC

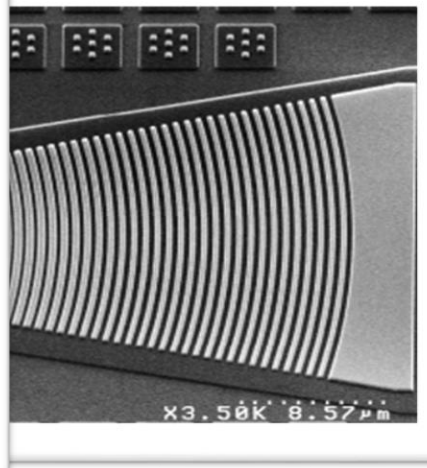
[1] P. Martin et all "Modeling of Silicon Photonics Devices with Verilog-A", MIEL 2014

WORK FLOW MPW WITH EUROPRACTICE







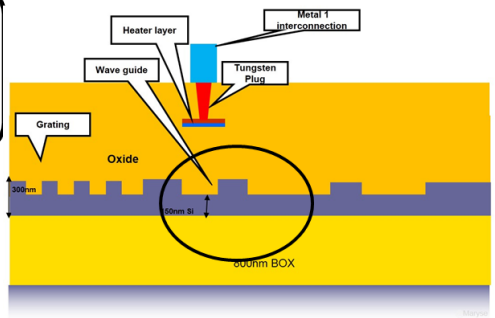


			Heater technologies with metallization	
			Minimum area: 2 regular full blocks	Minimum area: 5 regular full blocks
Die size	Regular (25 samples)	Full BLOCK (6 x 4 mm²)	28 650 €	21 500 €
		Half BLOCK (6 x 2 mm²)	14 325 €	10 750 €
	miniPhotonics (15 samples)	1 miniBLOCK (4 x 2 mm²)	9 550 €	NA
		2 miniBLOCKs (4 x 4 mm²)	19 100 €	NA
		Larger size	Contact us	Contact us
Options		Deep rib 65 nm	+ 1 765 €	
		Passivation opening	+ 1 765 €	
		Variable dose	included	included
		Metrology	included	included
		Dicing	included	included
		Fabrication report	included	included
		Final Resist cladding	included	included

Tape out through Europractice IC:

- **Q4 2016→ October 18th**

λ=1.31 µm TE mode



Devices	*Coupler 1D*	*Coupler 2D*	*Monomode Rib waveguide W400nm*	*Multimode Rib Waveguide*	HEATER Thermal efficiency
Performance	**IL < 2.5 dB loss**	**IL < 4,5 dB loss**	***Losses: < 2.5 dB/cm***	***Losses: < 0.3 dB/cm***	**0,5 > TE > 0,2 nm/mW**

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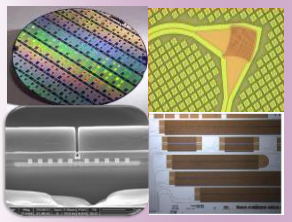
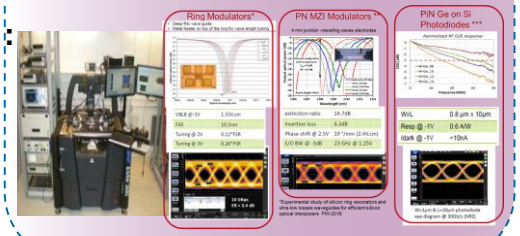
WORK FLOW MPW WITH CMP

LETI
- Mask preparation
- Adding Boarder for fabrication Tracking
- Adding dummies

Fabrication of Photonic circuit on CMOS 200mm Platform



Optical and Electrical Tests on test chips

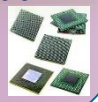


For Dicing & Packaging

Optical interconnects closer to the electronic chip :

CMP MPW wafer service
- Customer interface
- order form
- Support for design , Layout
- DRC

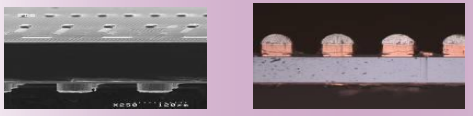
Dicing & Packaging



LETI

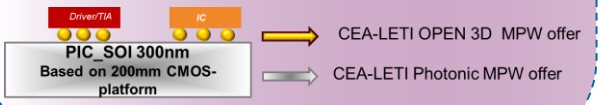
3D Technology implementation

Interconnections

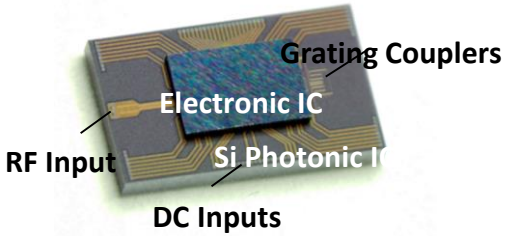


Metalization

Components stacking



Optional Packaging: Tyndall



Example of Final realization: EIC & PIC
Tyndall assembly

OPEN 3D
BOOST YOUR INNOVATION

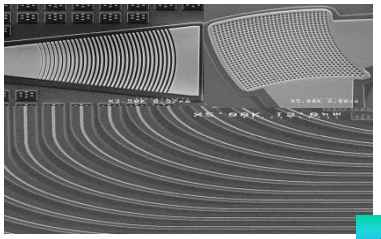
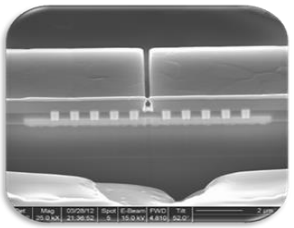
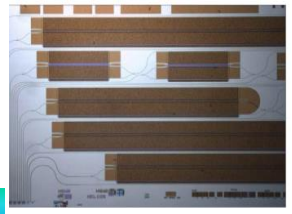
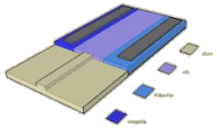
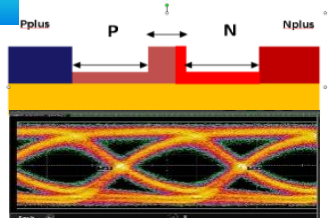
Our MPW offer is 3D compatible

Booth # 397 @ ECOC

GLOBAL LETI MPW OFFER ON

λ=1.31 µm TE mode **(310nm /800nm)**

NEW SOI PLATFORM!

Passives components	Heaters	Lateral Ge PIN diode	Carrier depletion PN MZ or RR Modulator
			
Si310-PH		**Si310-PHMP2M**	
Coupler 1D **IL < -2.5 dB loss** ***Coupler 2D*** **IL < -4,5 dB loss** *Monomode Rib waveguide :* ➢ ***Losses: < 2.5dB/cm*** *Multimode Rib Waveguide:* ➢ ***Losses: < 0.3dB/cm***	➢ **Thermal efficiency:** **0,5 > TE >0,2 nm/mW** ➢ **Sheet resistance:** **5 ,5 ohm / Sq**	 ➢ **Responsivity: > 0.75A/W** ➢ **Dark current: < 10nA @ -1 V** ➢ **Bandwith -3dB in S21 @ -1V : 30 GHz**	 ➢ **Vpi.Lpi < 2,5 V.cm** ➢ **Prop Loss < 2 dB/mm** ➢ **Data Rate up to 25Gbps**

Sign in October 18 th 2016 through
http://www.europractice-ic.com
SiPhotonics_technology_LETI_passives_w_heater.php

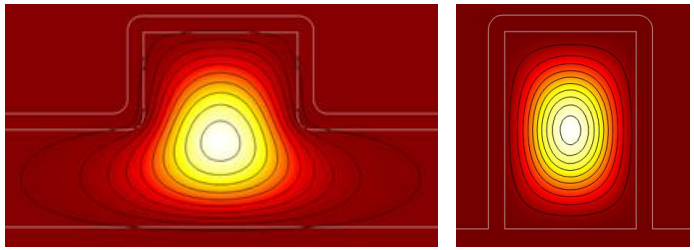
Si310-PHMP2M sign in Q4 2016

- Very high performance building blocks for λ=1.31 µm and later λ=1.55 µm
- Compatible Photonics and process 3D from CEA-LETI for Electronics integration
- PDKs with models available via Cadence, Phoenix software, and Mentor Graphics
- Technology compatible design rules with **300 mm industrial foundry***

Booth # 397 @ ECOC

Thick-SOI: Low loss in small footprint

In thick Si waveguides light is extremely well-confided into Si:



SM rib waveguides

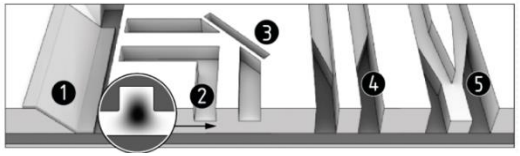
MM strip waveguides

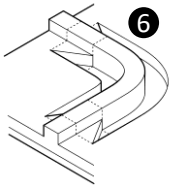
Light can be coupled between SM and MM waveguides without launching higher order modes

- Benefits of “Thick-SOI” (3...12 µm SOI)
  - Low optical losses
  - Ultra-dense integration
  - Dual-polarization operation
  - Tolerance to high optical power
  - Ultra-broadband SM operation
- Main applications in the short term:
  - Datacom / telecom *(Data centers etc.)*
  - Imaging *(OCT, LIDARs etc.)*
  - Sensing *(safety, security, environment etc.)*

PICs on 3 µm SOI wafers

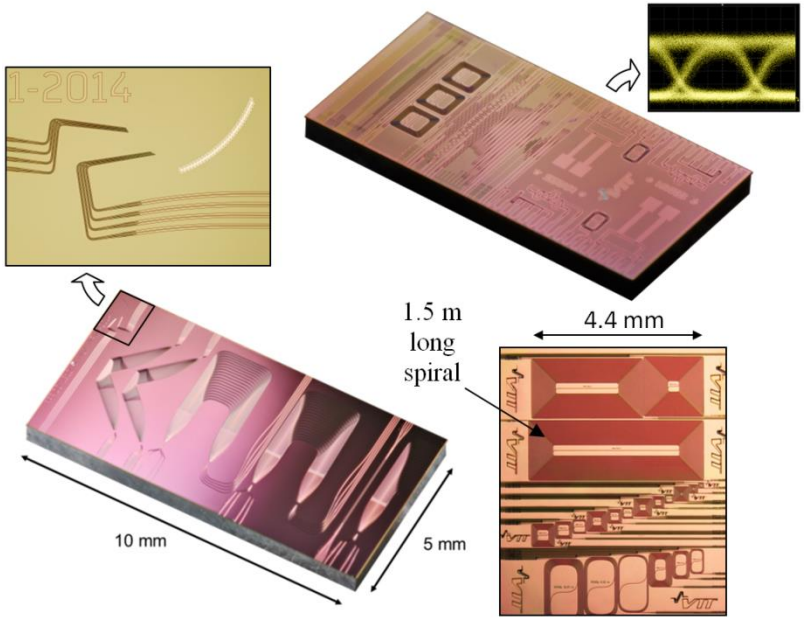
- Library of passive building blocks, heaters, switches and (slow) modulators available via MPW runs *(contact silicon.photonics@vtt.fi)*
- High-speed active components developed for customer needs
- PDKs available (PhoeniX, IPKISS)

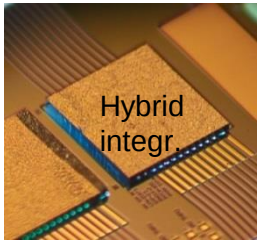


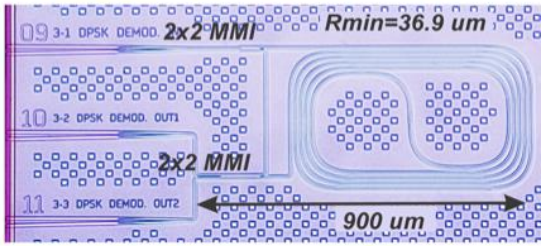


Bending radius down to 1 µm!

1. Metal mirror
2. Rib waveguide
3. TIR mirror
4. Rib-strip converter
5. Vertical taper
6. Euler bend





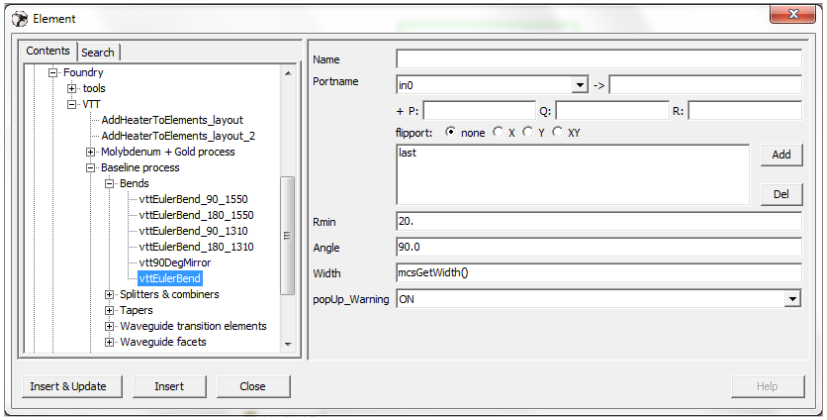


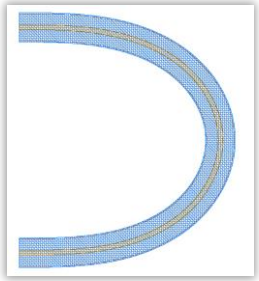
VTT PDK

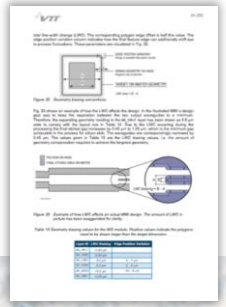
VTT and PhoeniX Software announce a process design kit to support silicon photonics developers around the world

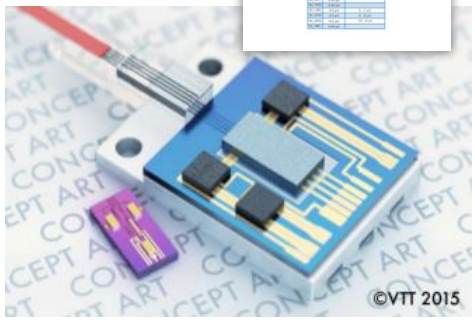
22/08/2016

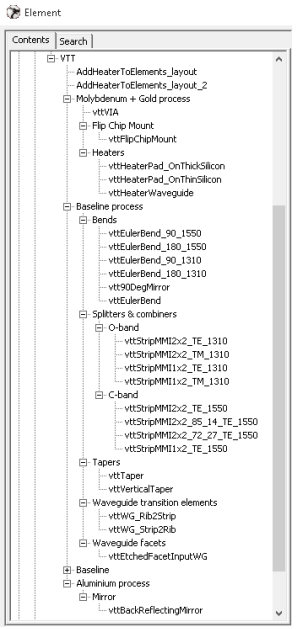
Creation of a mature and validated PDK, sponsored by Actphast





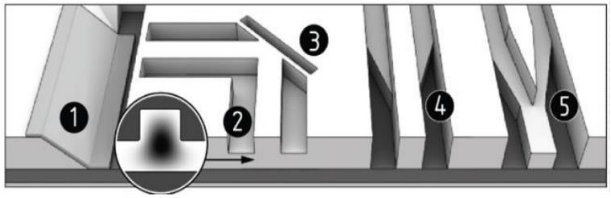






- New building blocks
- Better design rules
- Add models for circuit simulation
- Include process information for yield and sensitivity analysis

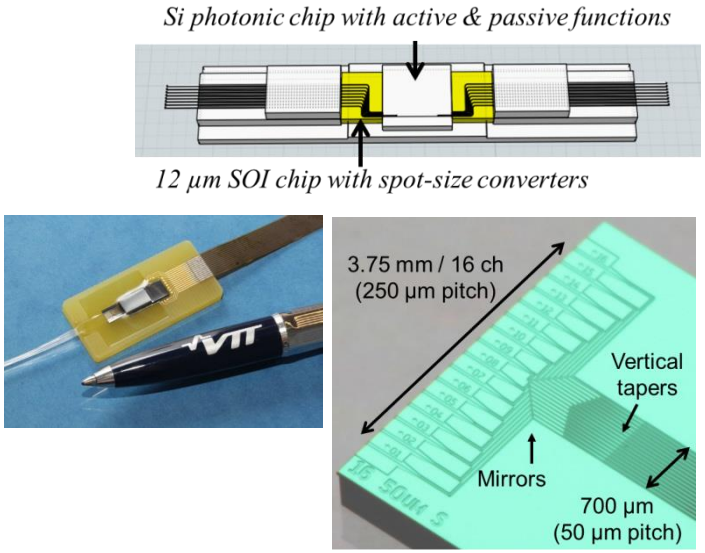
ACT PHAST — Access Center for Photonics Innovation Solutions And Technology Support

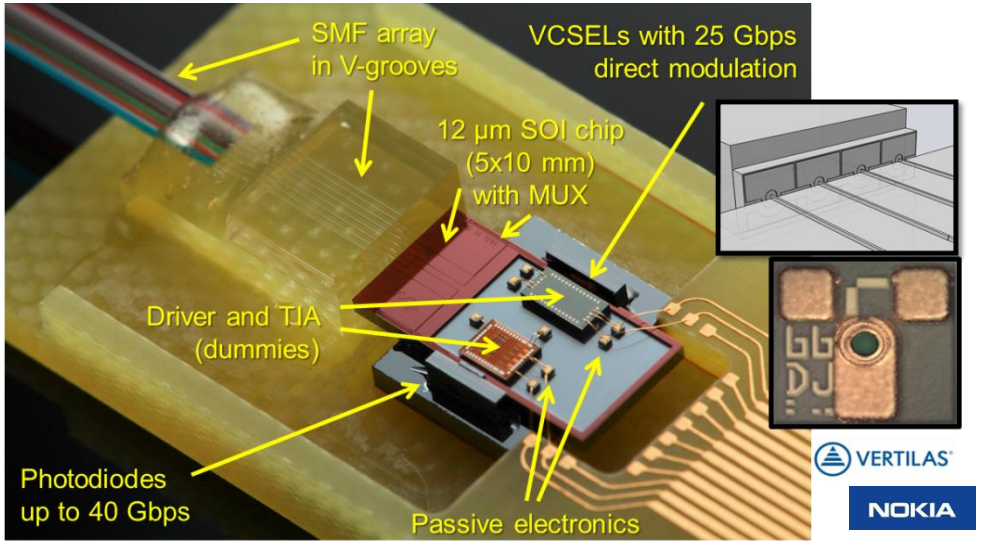


(C) 2015. ALL RIGHTS RESERVED. PHOENIX SOFTWARE.

Interposers on 12 µm SOI wafers

- Excellent coupling to standard SM fibers (SMF-SOI-SMF loss 1 dB)
- Spot-size and pitch converters to couple into small-waveguide PICs
- Scalable to attach >100 fibers, VCSELs, PDs etc.
- Mirrors with <0.3 dB/90° loss



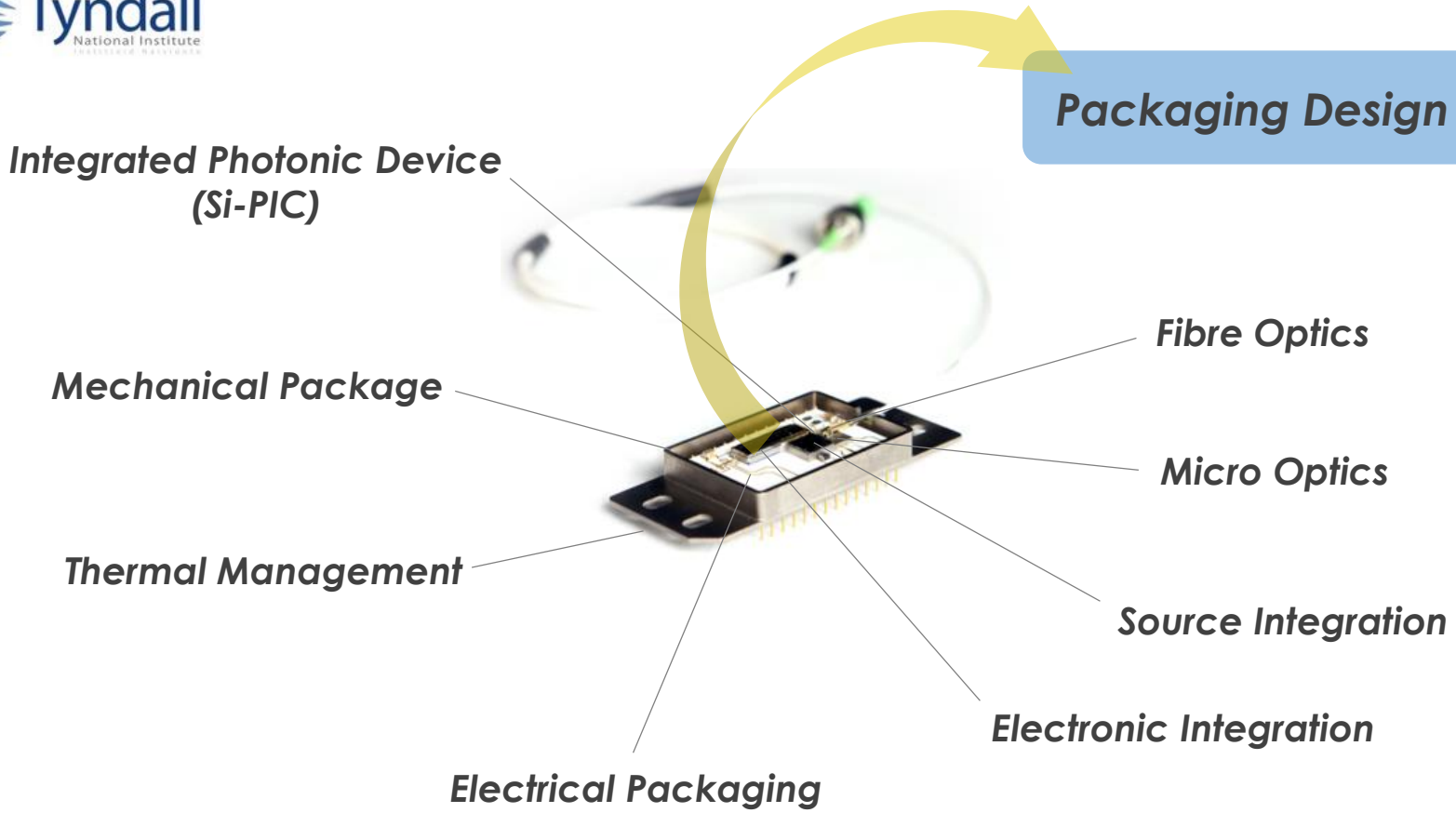


Outline

- Recent developments by silicon photonics design tool developers
  - Luceda IPKISS
  - PhoeniX
- Updates from the technology providers
  - imec
  - IHP
  - LETI
  - VTT
- Packaging service at Tyndall and design service by VLC Photonics

Complete Packaging Foundry Service

Tyndall National Institute



Packaging Design Rules

Tyndall National Institute

TYNDALL NATIONAL INSTITUTE

Silicon Photonics Packaging Services for EuroPractice-MPW runs

Prepared by: Photonics Packaging Group (Tyndall National Institute)
Prepared for: EuroPractice (Silicon Photonics)
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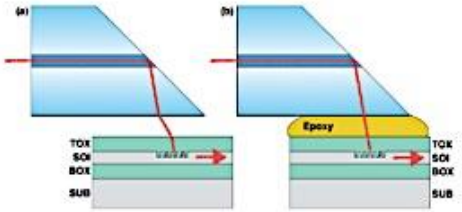


Figure 4 For GPC, adding index matching epoxy does not change the AOI of light incident on the grating-coupler.

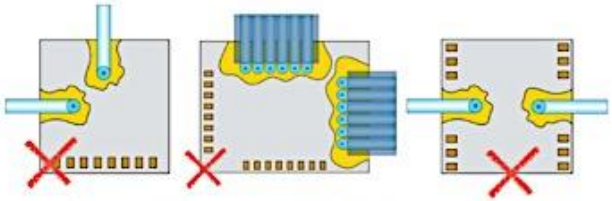
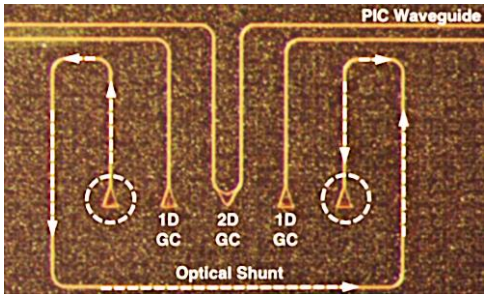
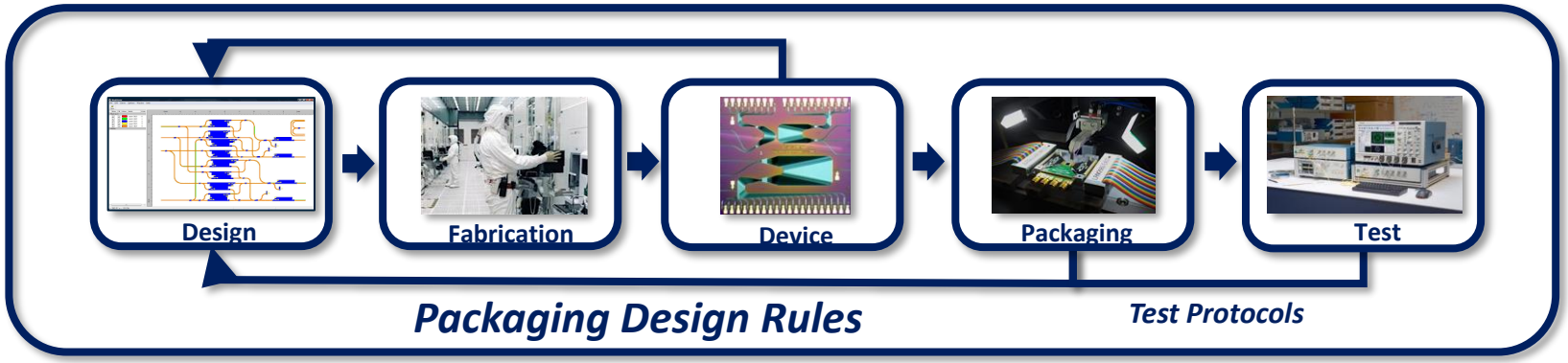


Figure 7 - Schematic showing PIC designs that are incompatible with the EuroPractice packaging offered by Tyndall. Orthogonally orientated single-fibre or fibre-array GPCs are not permitted, and fibre-coupling cannot be made from an PIC-edge that also needs wire-bonding.



Packaging Design Rules & Manufacturing

1. Device Layout Rules



2. Package Design
3. Packaging Materials
4. Packaging Equipment (Tooling)
5. Pre- & Post-Package Test Protocols
6. Outreach & Training (software development)

European PIC Pilot Lines

Design house contributions (I)

Consultancy

Model system & simulate performance

Select best material substrate

Map functionalities into devices

Match devices into fab platforms

Evaluate providers and related IP

Techno-economic studies

Design house contributions (II)

Design services

Map devices into building blocks

Design new building blocks or adapt existing ones

Place building blocks into layout and route all connections

Ensure good packaging and test practices on the design

Clean any errors according to foundry design rules

Provide design support to customers

Design house contributions (III)

Test services

Bare die & device characterization

Optical & electrical measurements

Thermal testing and wirebonding

Design house contributions (IV)

Packager Brokers

- From 1-10 units to high volume
- Wirebonding and flip-chip
- DC and RF, thermal control
- Fiber pigtailing, arrays
- Standard and custom housings

Software Brokers

- Mode solving
- Mode propagation
- Circuit simulation
- Layout

Foundry Brokers

- All main substrates: Si, SiN, PLC, InP, GaAs, Polymer
- +20 validated photonic foundries
- MPW runs (ePIXfab/EUROPRACTICE, JePPIX, etc.)

Summary

- Photonic design tools developers are working together to provide improved design flow
- Access to technology platforms with thin and thick SOI with variety of passive and active components in their component libraries
- Tyndall is working towards the development of pilot line for packaging

Thanks for your attention